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MS-7733

Mini ITX

Ver: 2.1

Intel -MahoBay plamform Z77

CPU:

IVY bridge LGA1155

System Chipset:

Panther Point

Onboard Chip:

HD Audio Codec:ALC892 colay ALC887

LAN-RTL8111E

SIO:Fintek F71889AD

Flash ROM: SPI 64 MB

Main Memory:

*DDRIII (800/1066/1333MHz) * 2 (Dual Channel)*

ACPI:

UPI

PWM:

VRD12 -UP1618E-6Phase

Expansion Slots:

*PCI Express (X16) Slot * 1*

Other: *SATA3.0 x2+SATA2.0 x2 (PCH)*
*USB2.0 *13*
*REAL USB3.0 *2*
*FRONT USB3.0 *2*

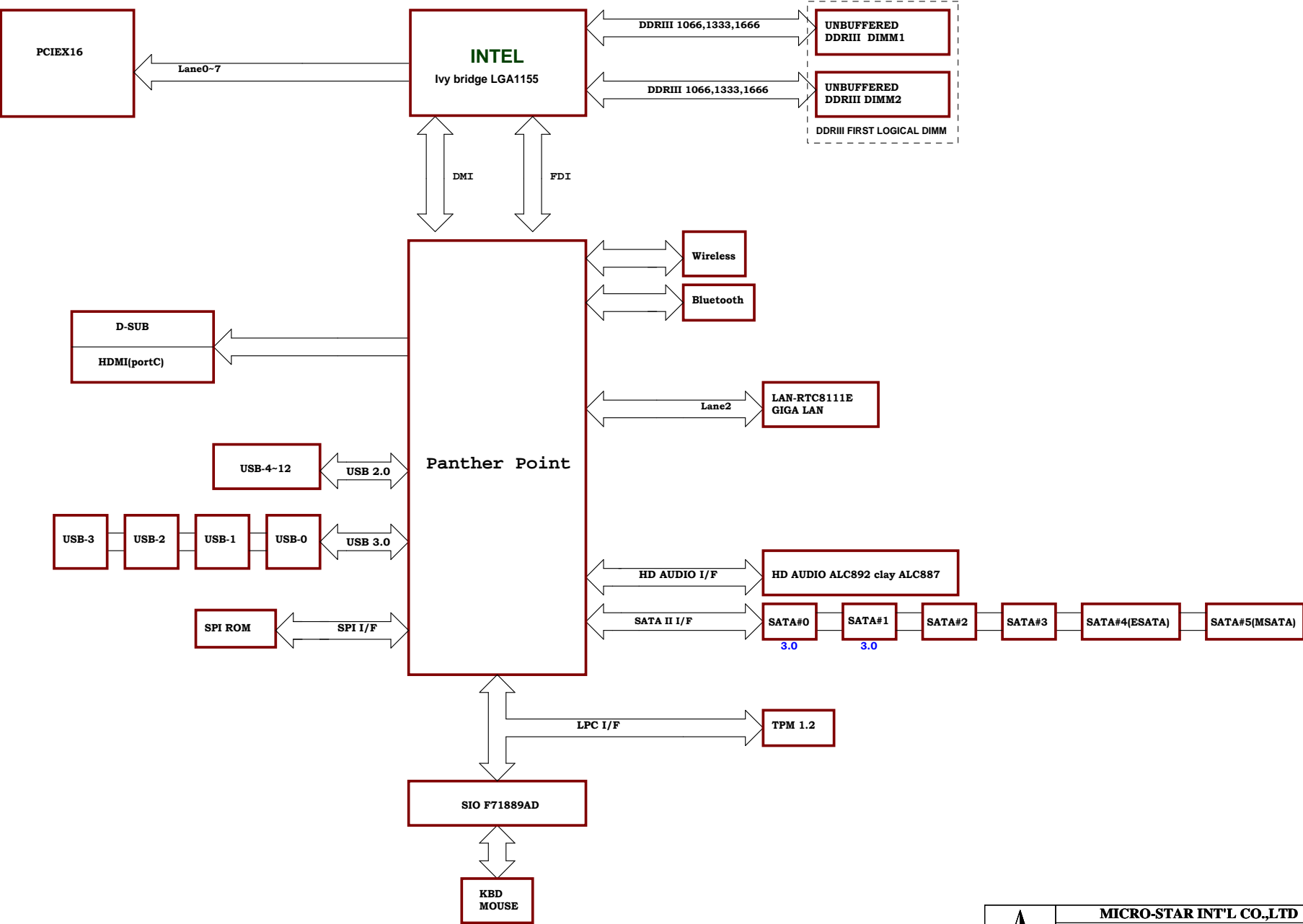


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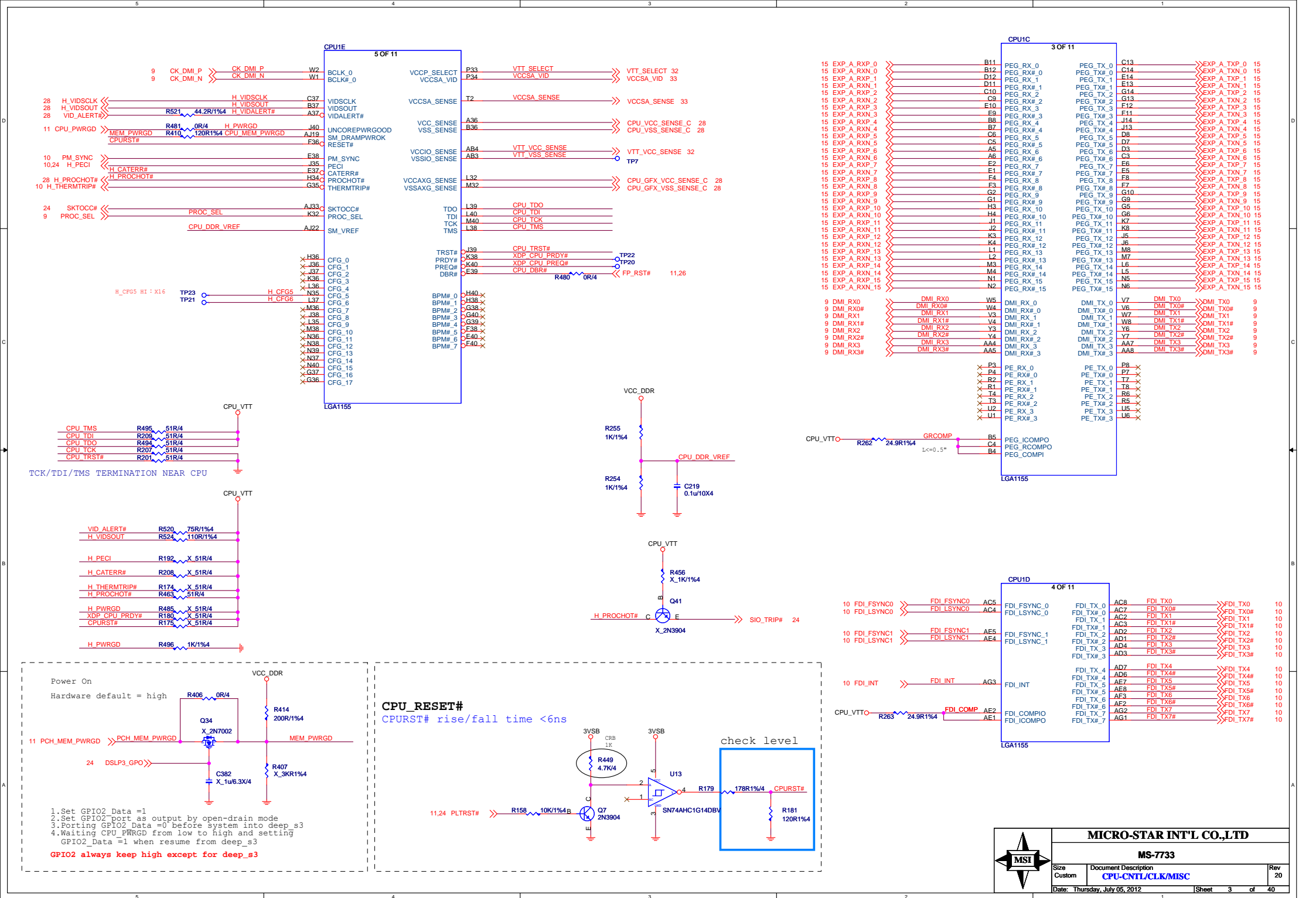
MS-7733

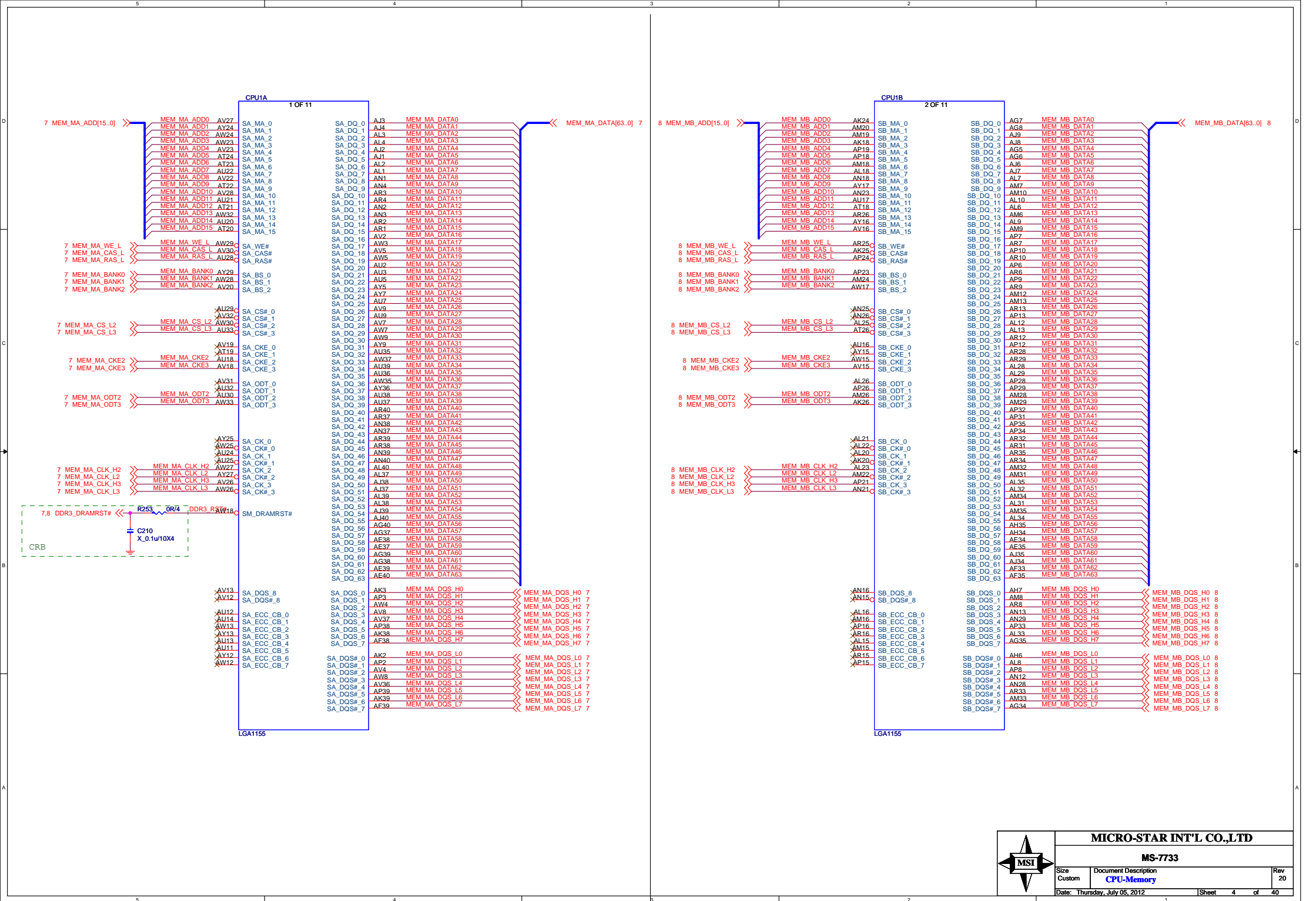
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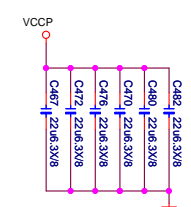
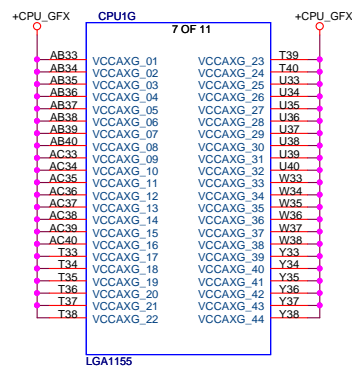
MS-7733 2.0 Block Diagram



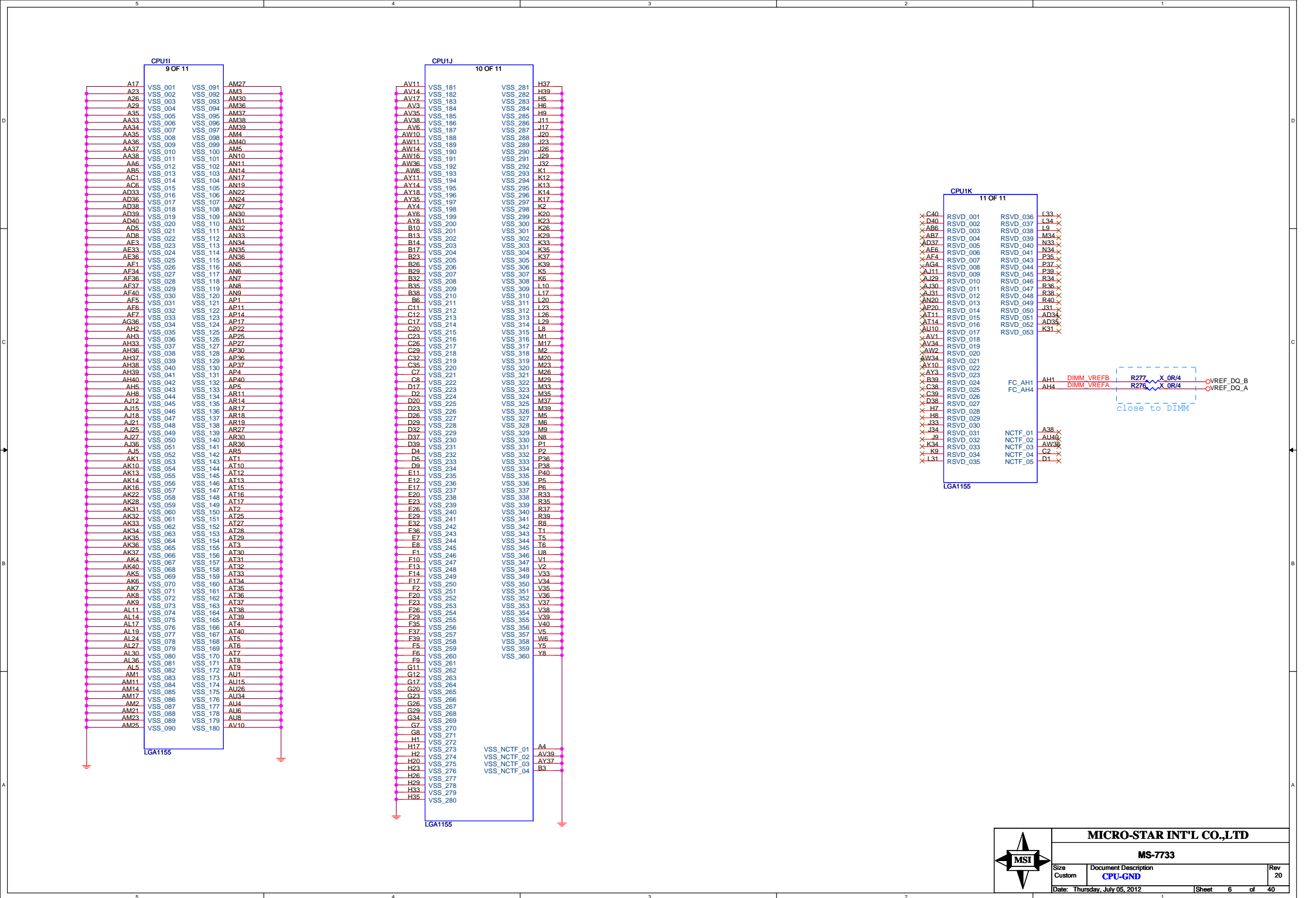
Slot Sequence:
PCIE X16





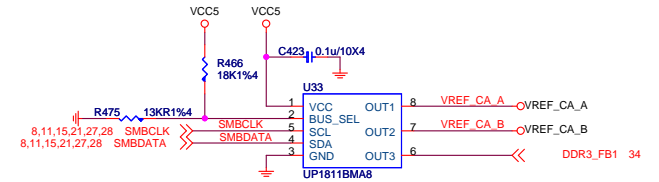
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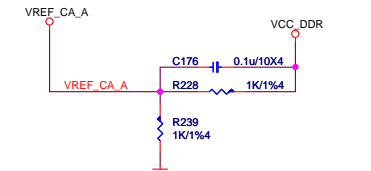


UPI VOLTAGE CONSOLE

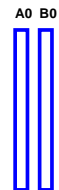
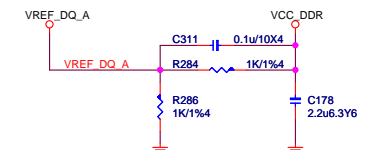
0x26:RH=18K,RL=13K



UPI VOLTAGE CONSOLE



UPI VOLTAGE CONSOLE



8 SMBCLK_DDR >> SMBCLK_DDR R12 >> SMBCLK 8,11,15,21,27,28
8 SMBDATA_DDR >> SMBDATA_DDR R11 >> SMBDATA 8,11,15,21,27,28



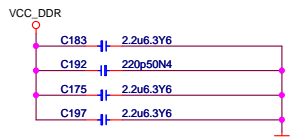
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MS-7733

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DDR3

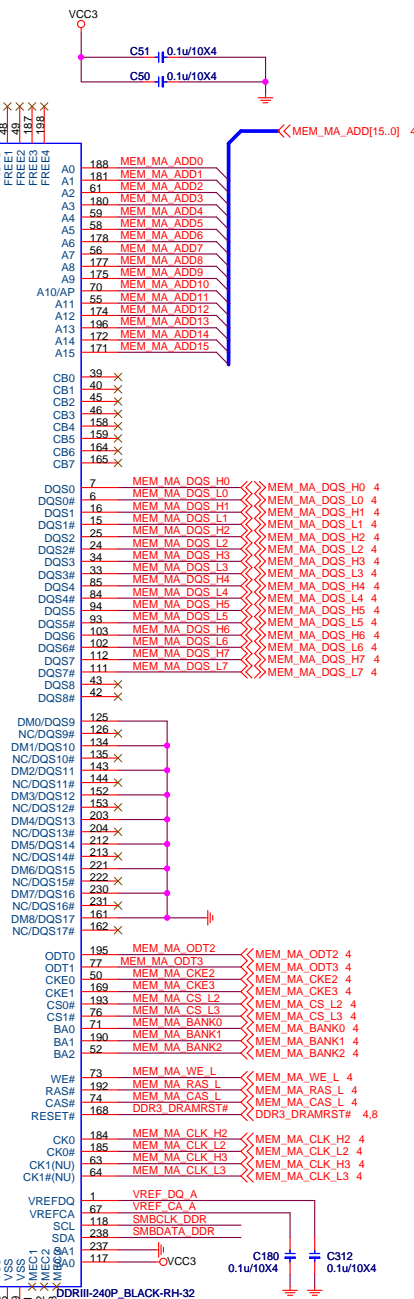
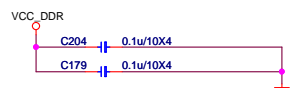
Place close to DIMM1



Place close to DIMM1 with DIMM2

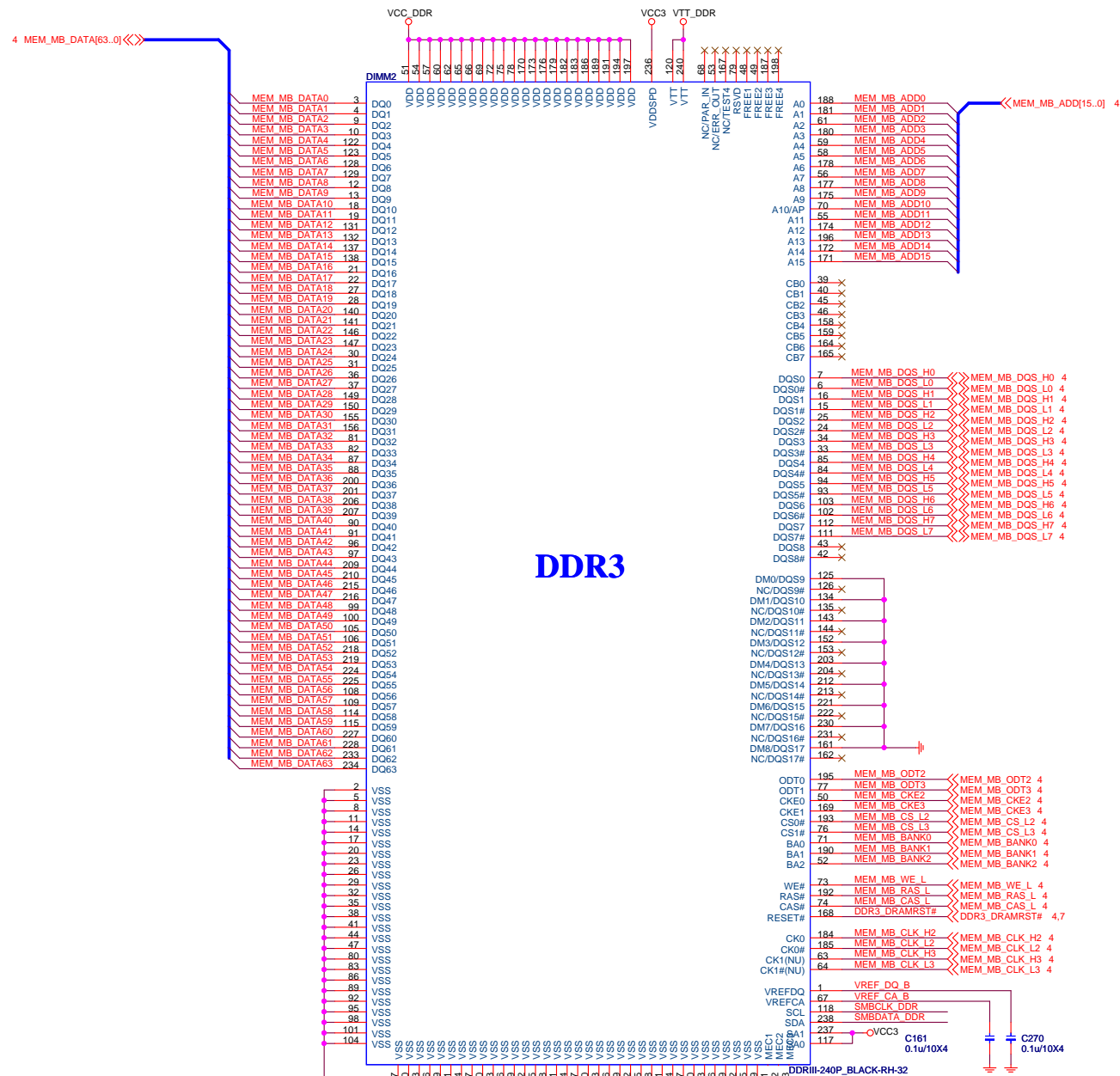


Place close to DIMM2



(CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]

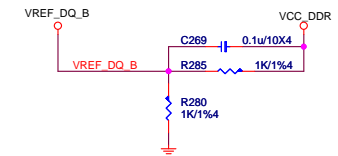
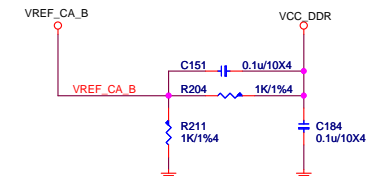
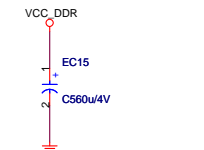
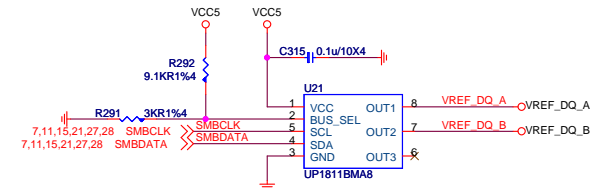
DDRIII DIMM_B0



(CHANNEL-B)
ADDRESS = 1:1 [SA1:SA0]

UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K



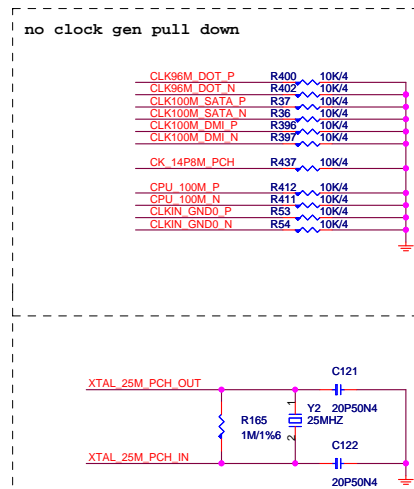
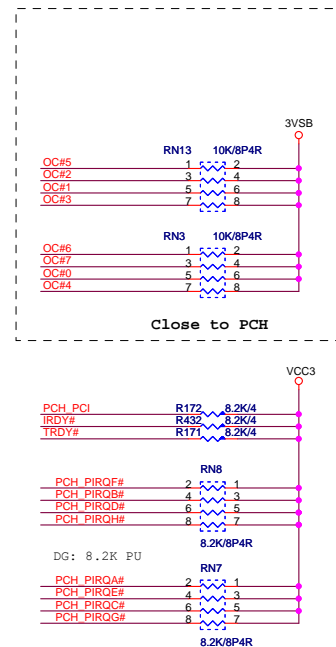
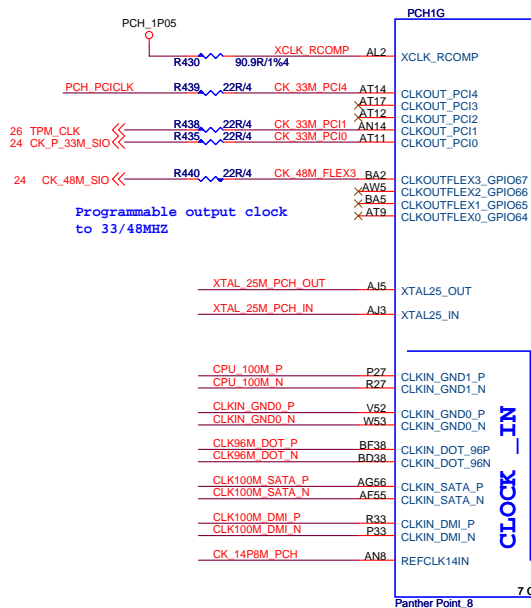
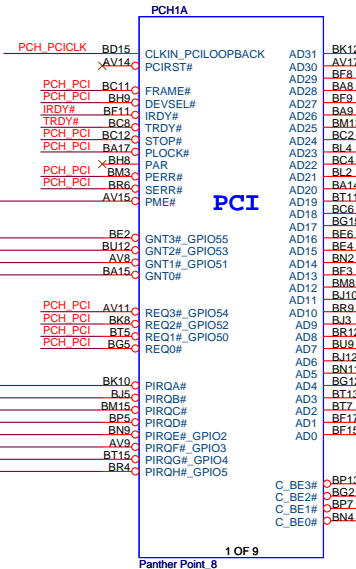
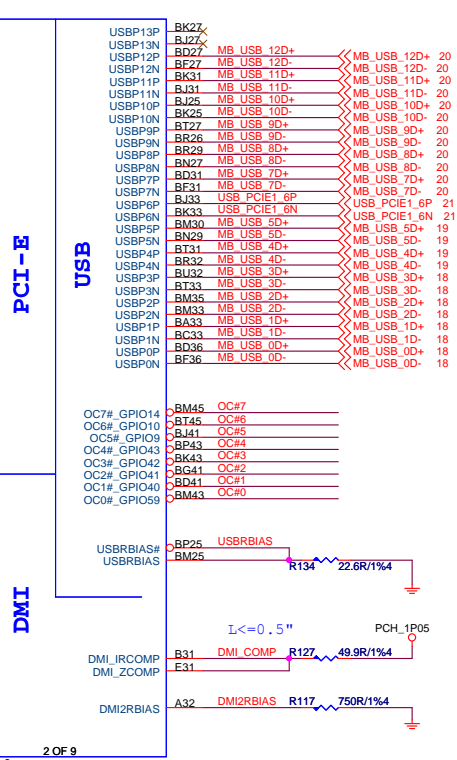
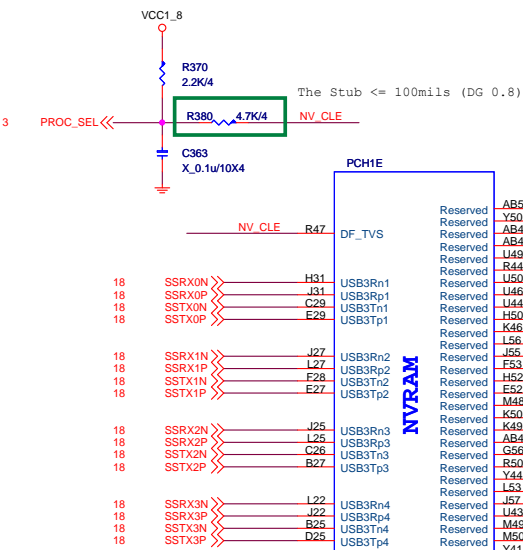
SMBCLK_DDR << SMBCLK_DDR 7
SMBDATA_DDR << SMBDATA_DDR 7

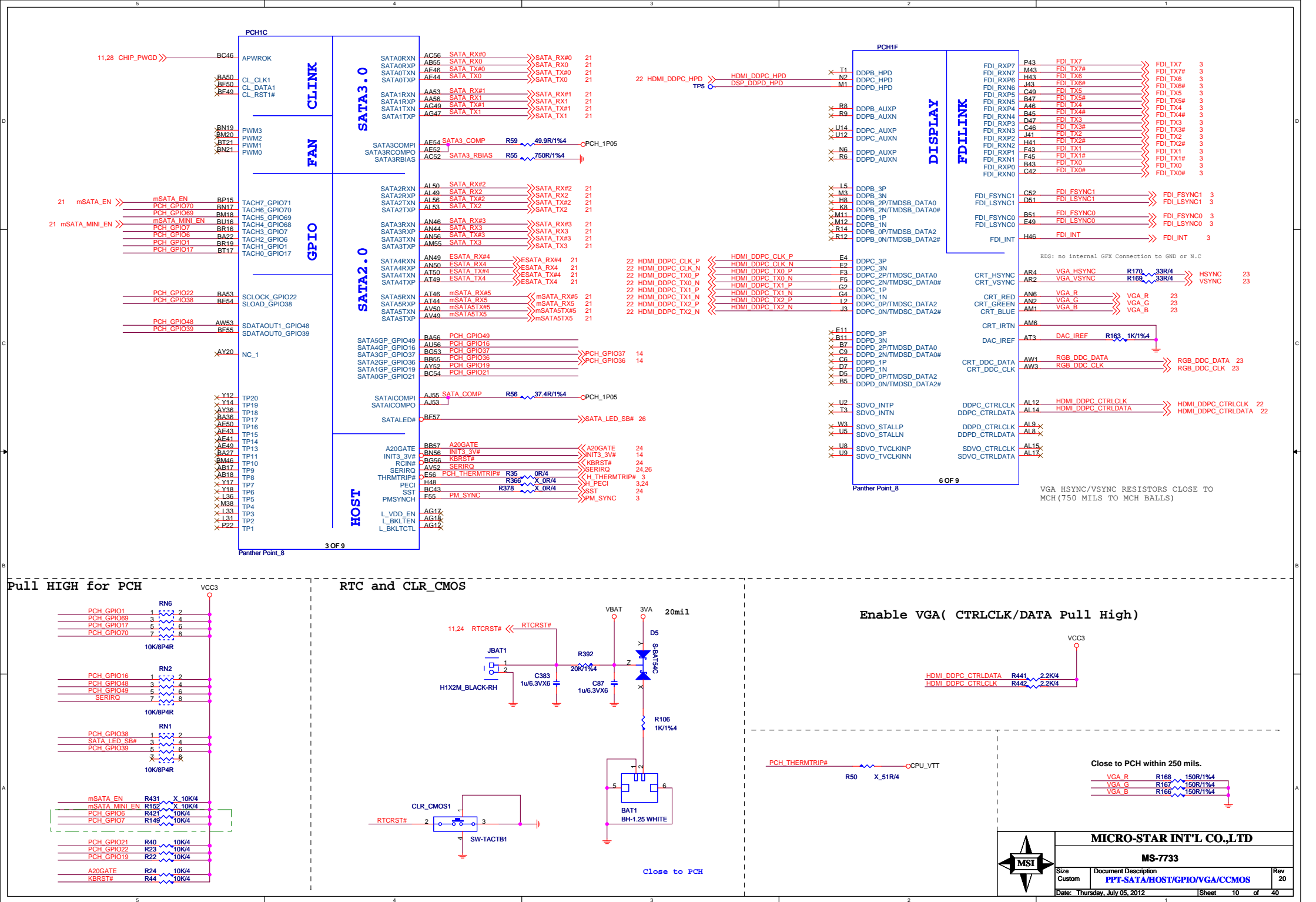


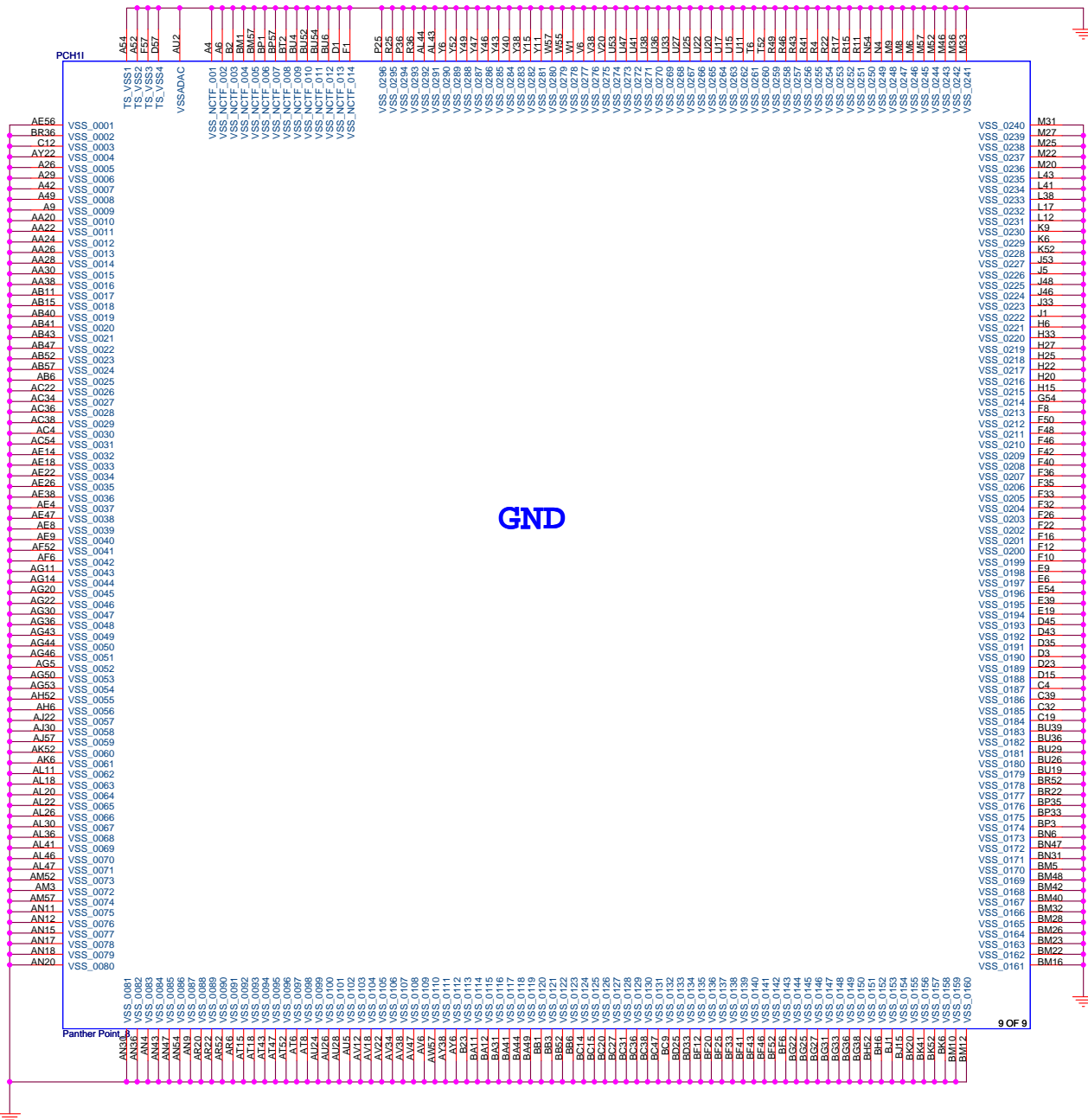
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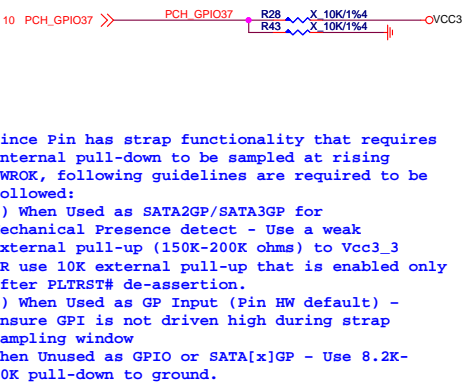
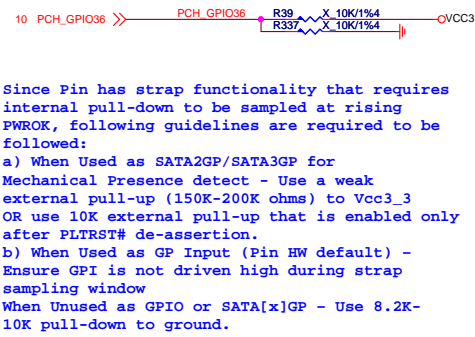
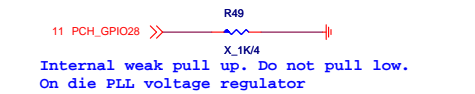
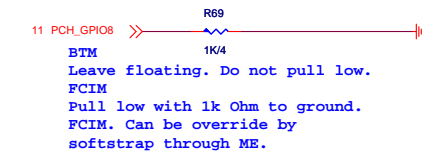
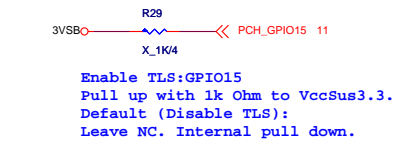
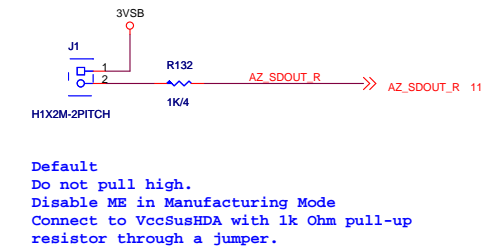
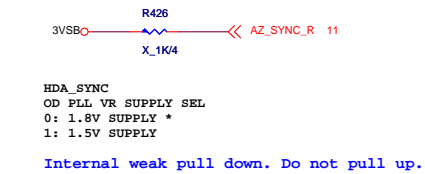
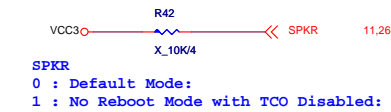
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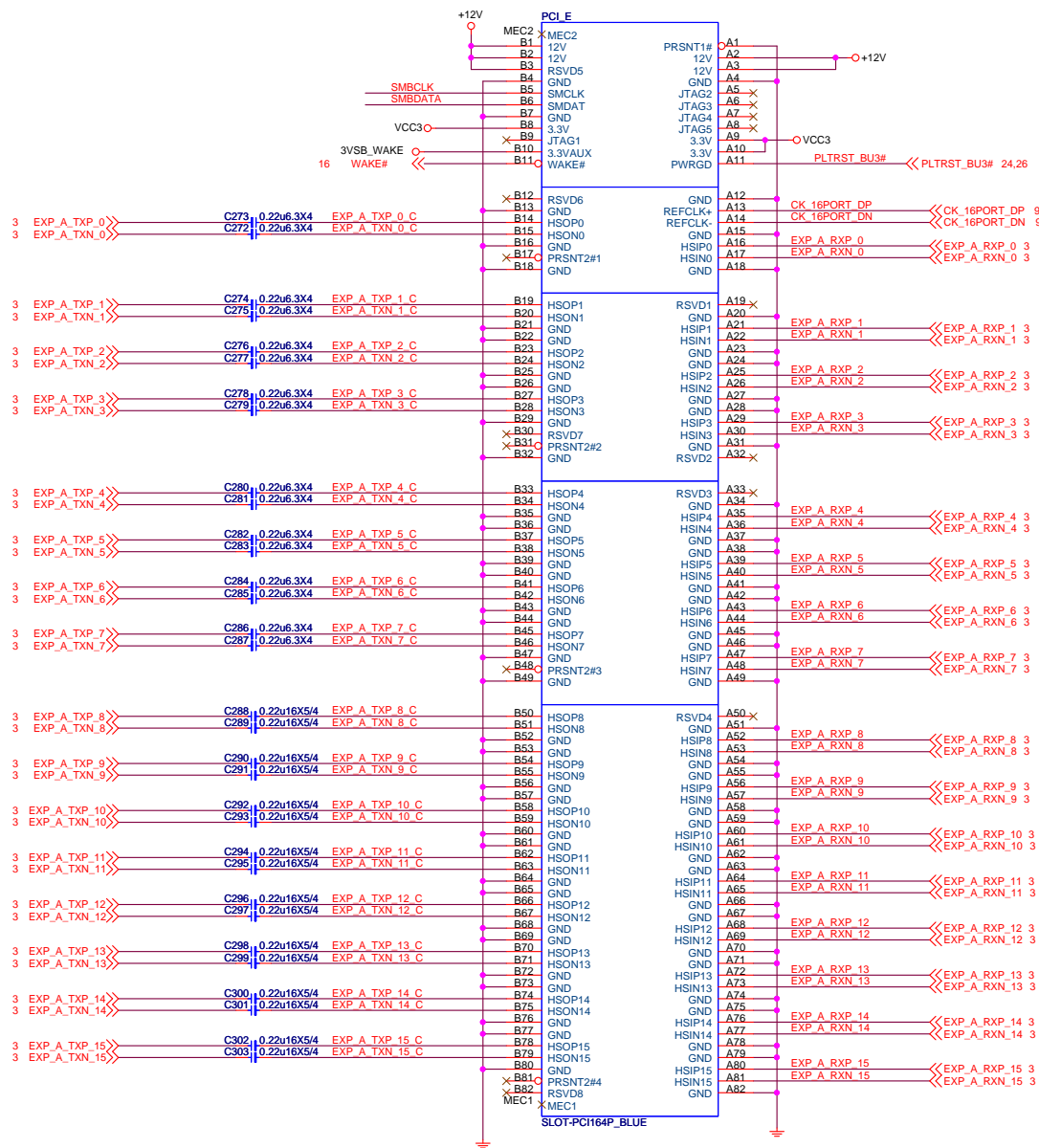




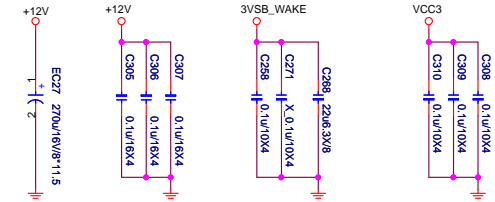


PCH Straps



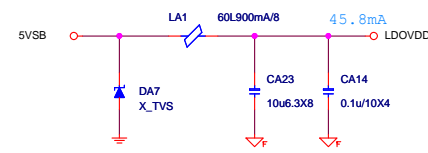
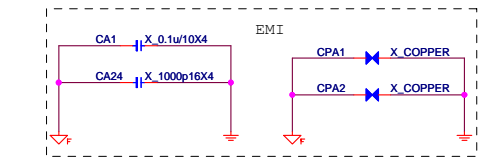
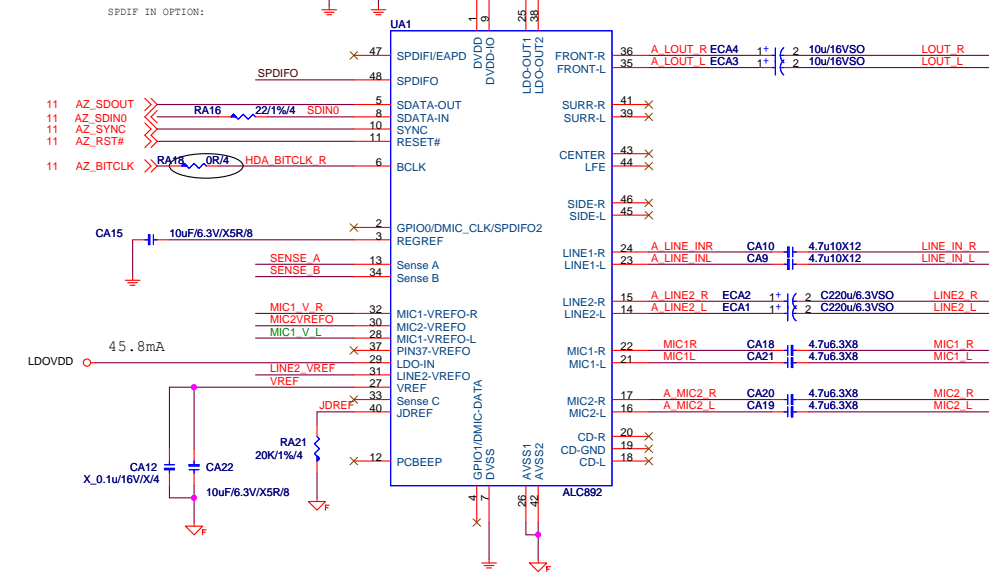


7,8,11,21,27,28 SMBCLK >>> SMBCLK
7,8,11,21,27,28 SMBDATA >>> SMBDATA

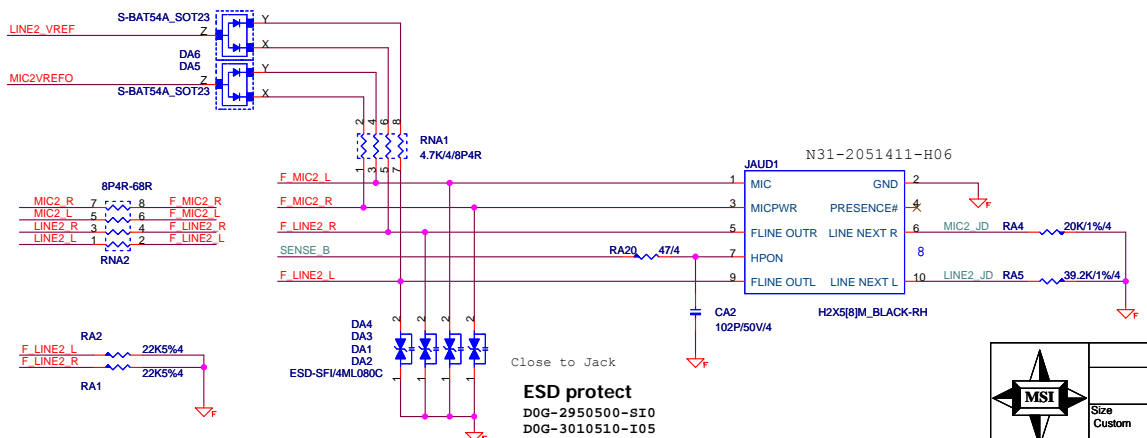
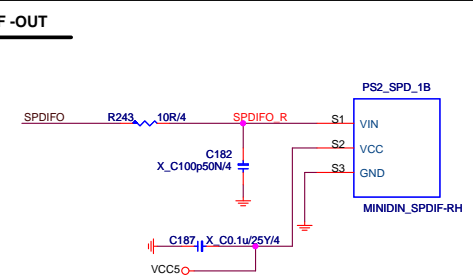
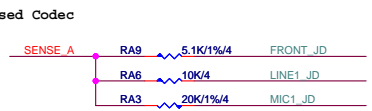


ALC887

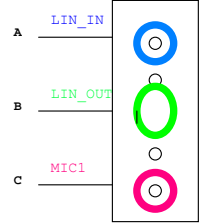
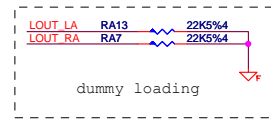
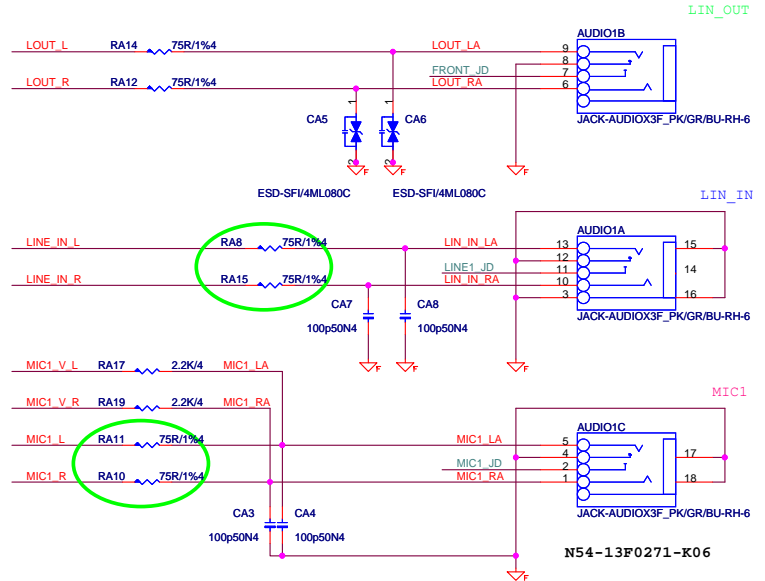
ALC892



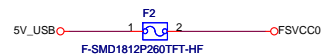
CA457,CA102 close to LA1



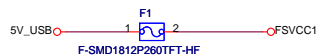
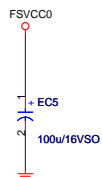
ESD protect
D0G-2950500-SI0
D0G-3010510-I05



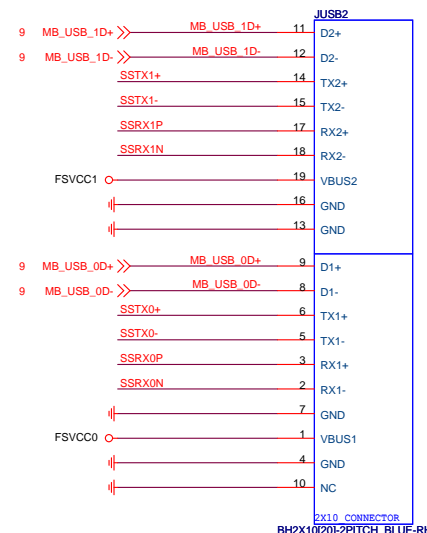
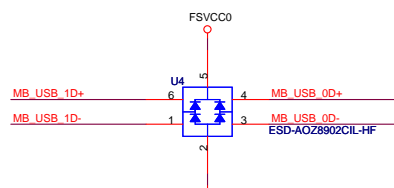
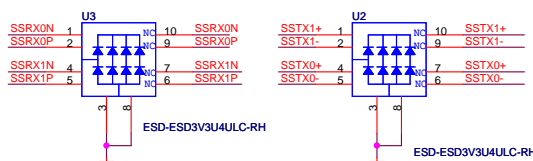
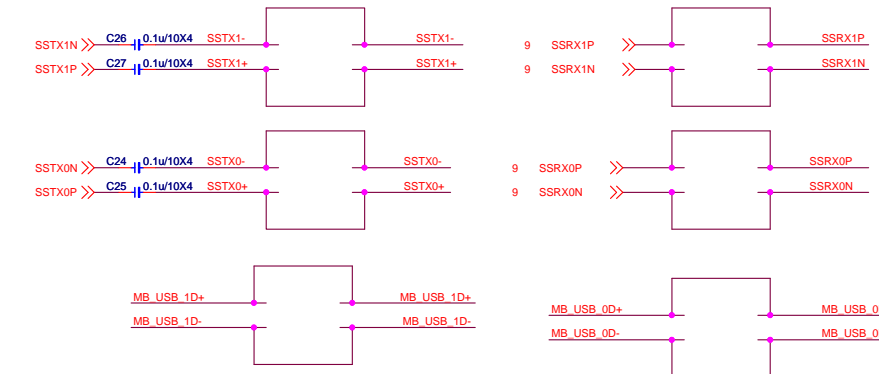
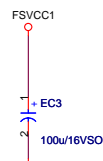
FRONT USB30 PORT 0,1



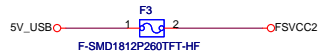
900 mA
min 40mil.



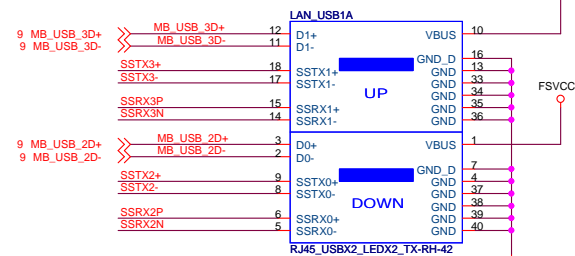
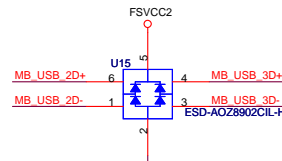
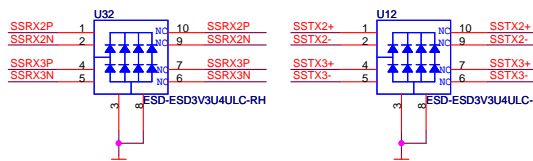
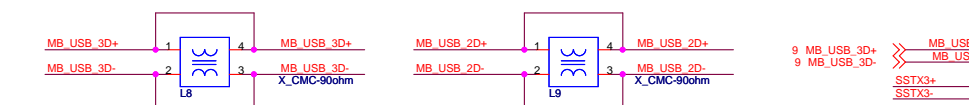
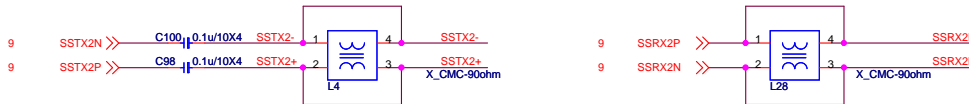
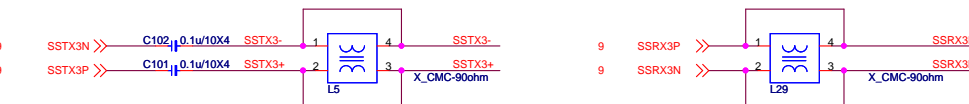
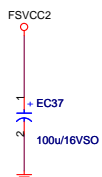
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min 40mil.



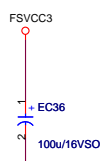
REAR USB30 PORT 2,3



900 mA
min 40mil.

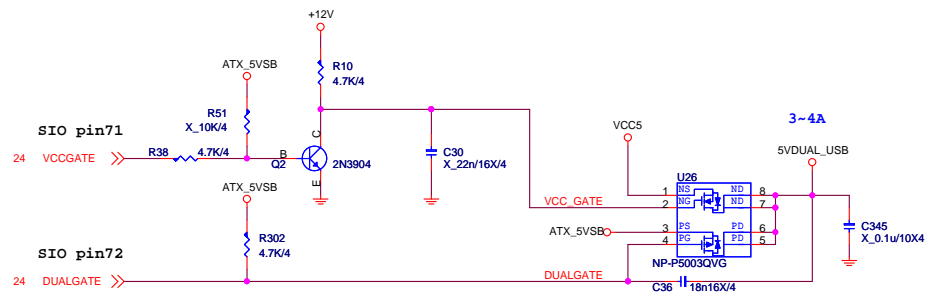


900 mA
min 40mil.



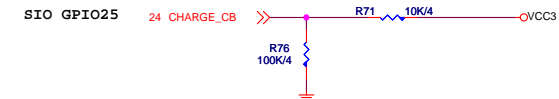
MICRO-STAR INT'L CO.,LTD		
MS-7733		
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5VDUAL_USB

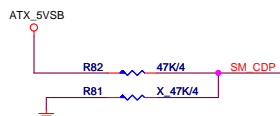
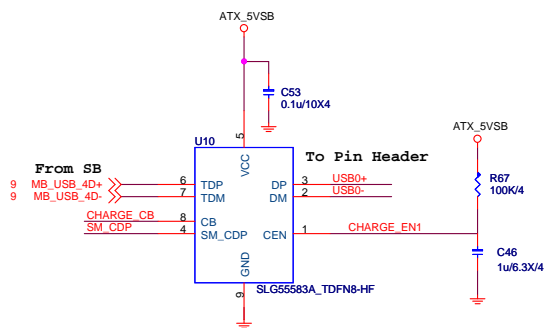
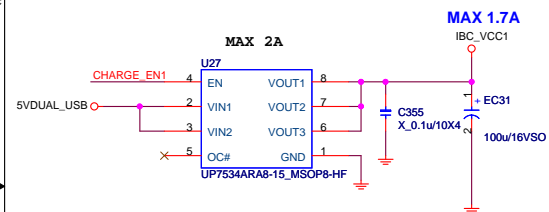


Update- 2010.7.15

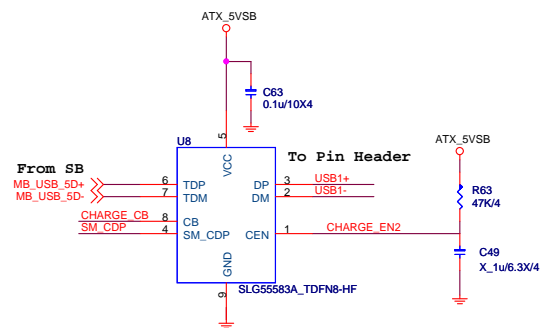
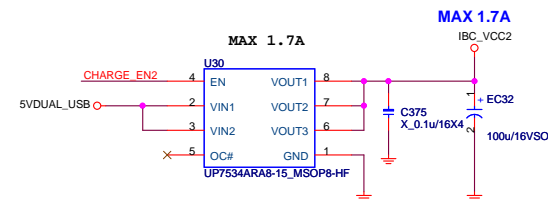
SIO GPIO40



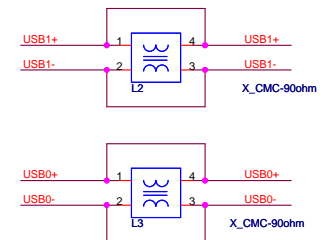
USB POWER PORT 0 For USB Charging



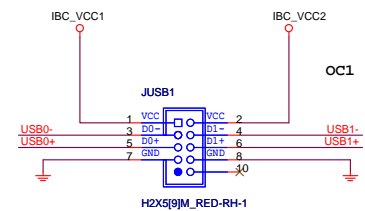
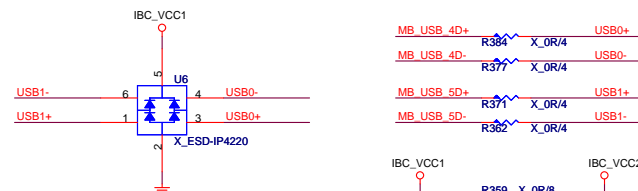
USB POWER PORT 1 For USB Charging



FRONT USB PORT 0,1



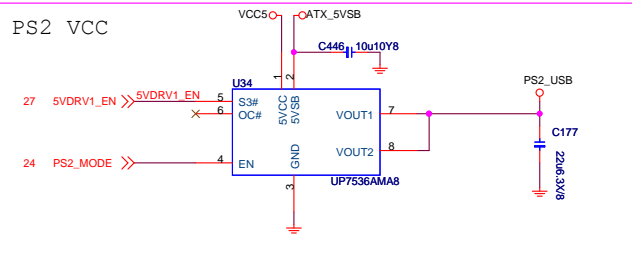
COLAY remove USB charger ic



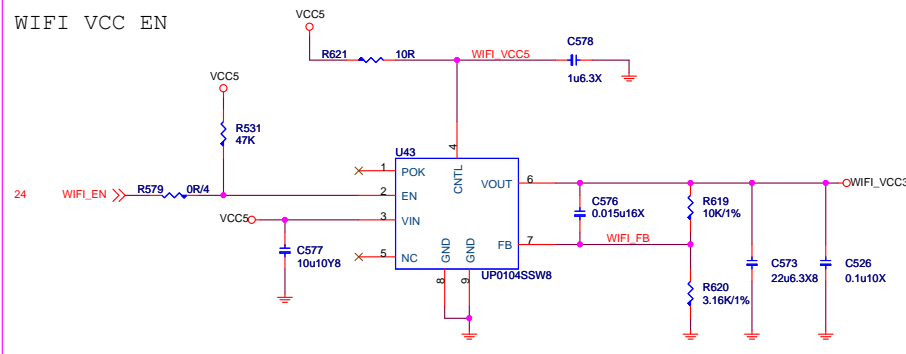
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MS-7733			
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Rear USB Connector

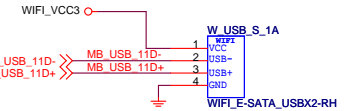
PS2 VCC



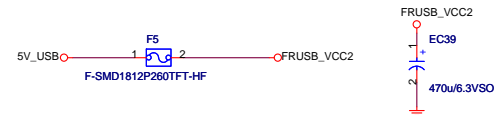
WIFI VCC EN



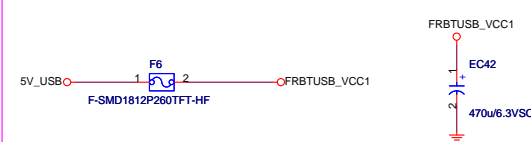
WIFI



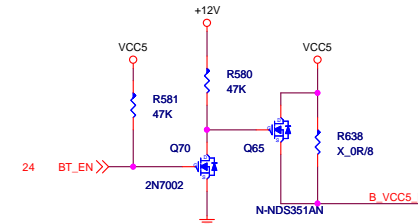
WIFI USB VCC



Bluetooth USB VCC

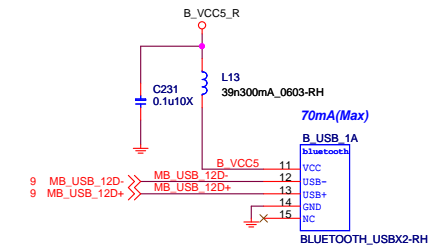


Bluetooth VCC EN

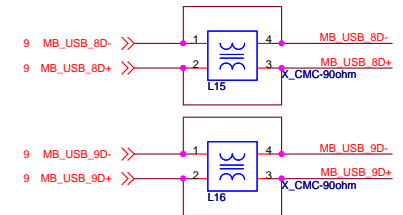


USB PORT 11,12(With BT & WIFI)

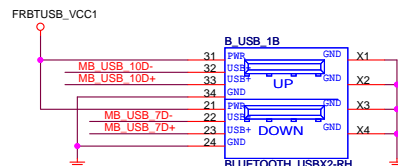
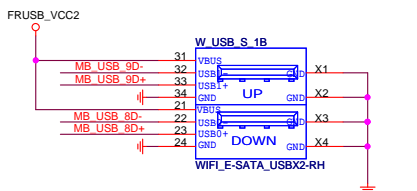
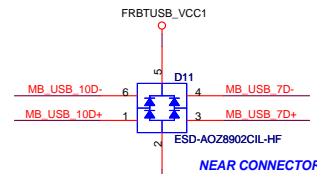
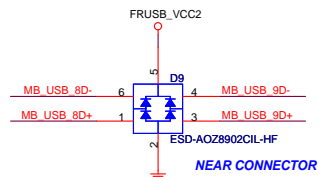
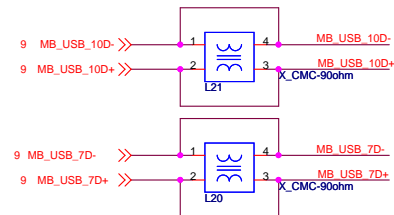
Bluetooth



REAR USB PORT 8,9 (With WIFI USB)

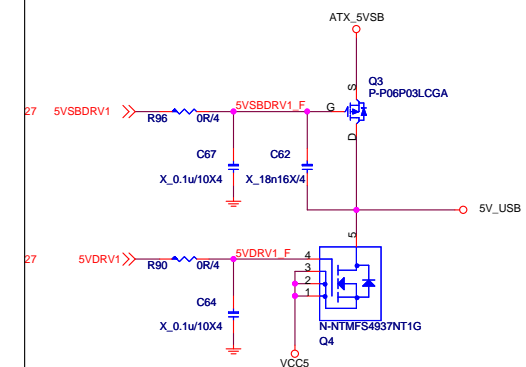


REAR USB PORT 10,7(With BT USB)



USB POWER

UP7501+MOS+FUSE



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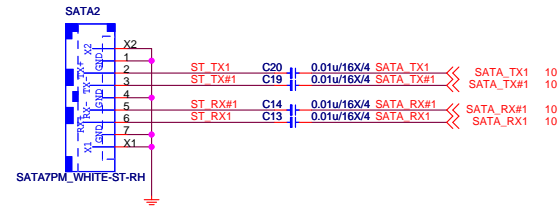
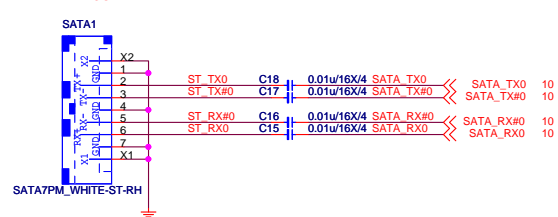
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Custom	Rear I/O & USB2.0 & BT	20
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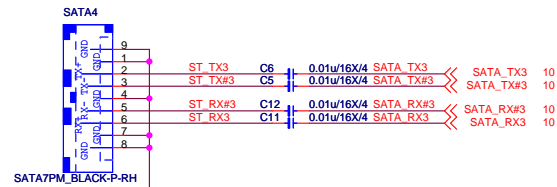
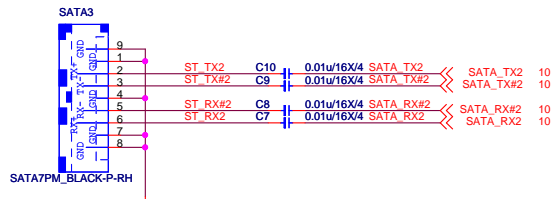
SATA1-2

3.0

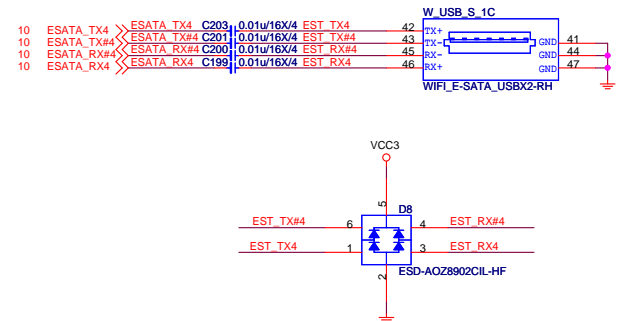
white



SATA3-4

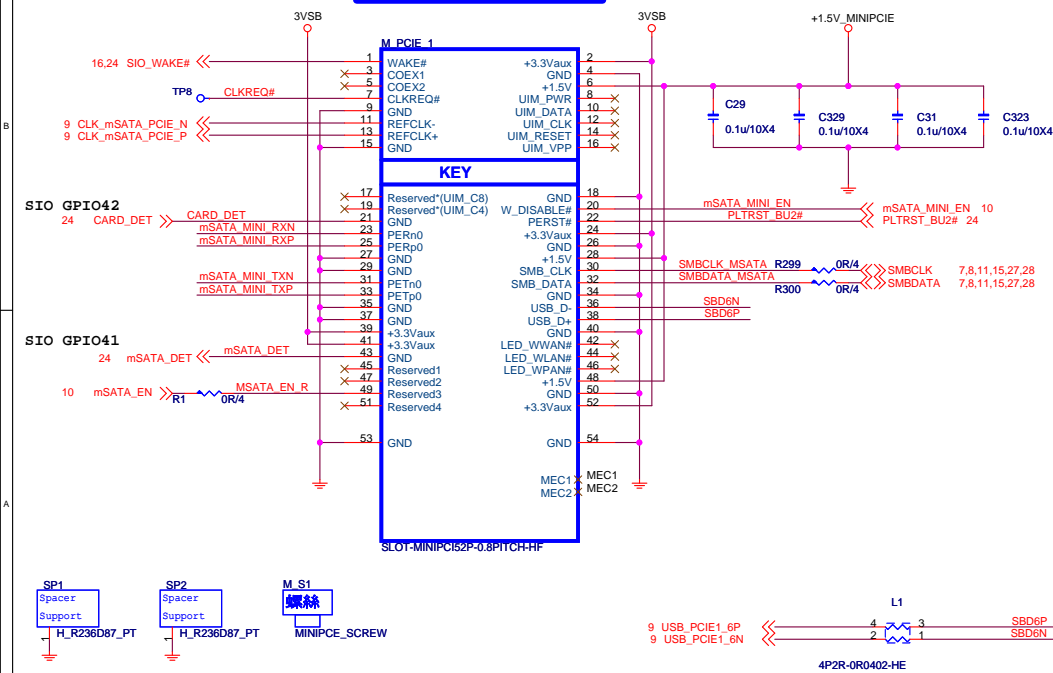


WIFI ESATA

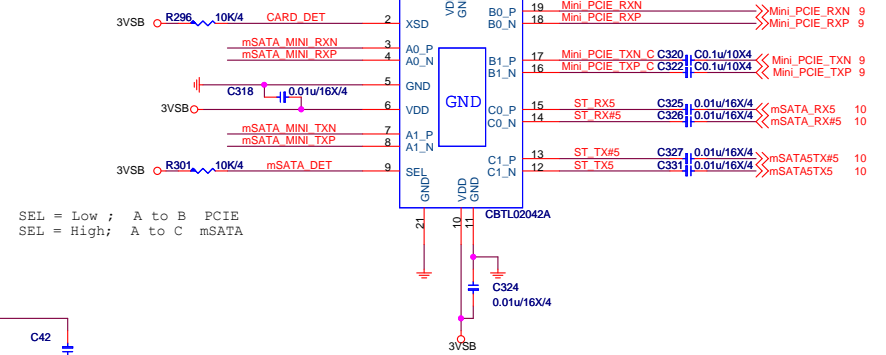


Mini PCIE LONG CARD

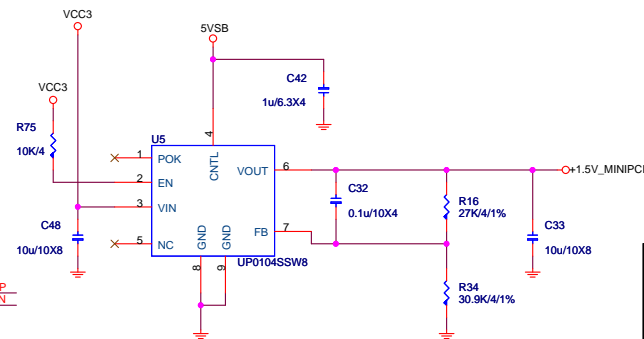
3VSB Mini PCIE, 1.5A



XSD = High; no device inserted
XSD = Low; device had inserted



SEL = Low ; A to B PCIE
SEL = High; A to C mSATA

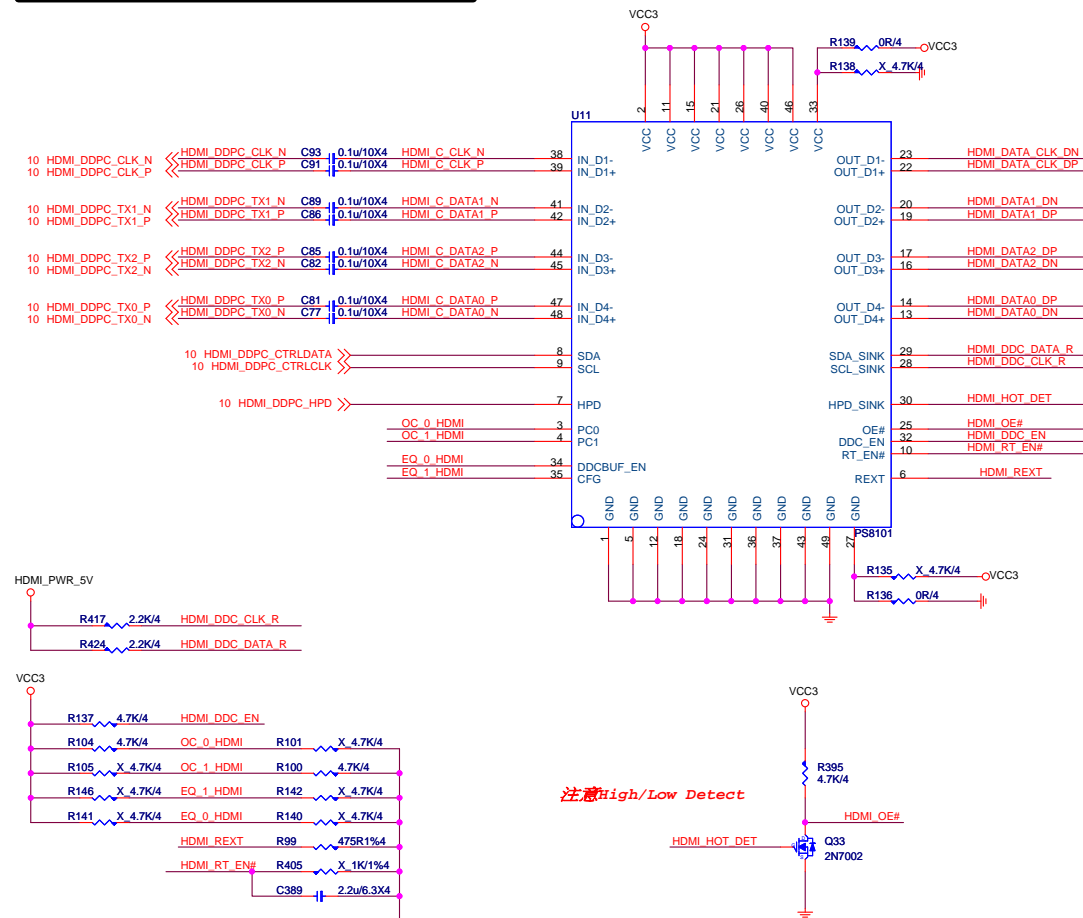


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HDMI level shifter



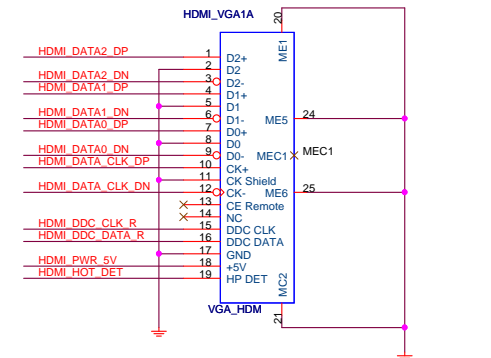
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

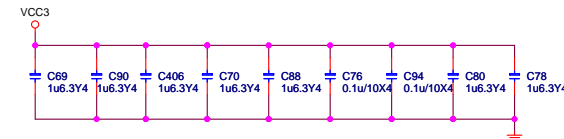
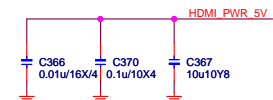
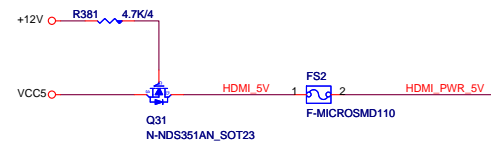
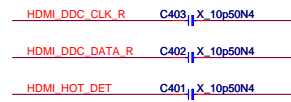
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_ON
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_OP
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI_B_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMI_B_CTRL_DATA	



EMI cap.





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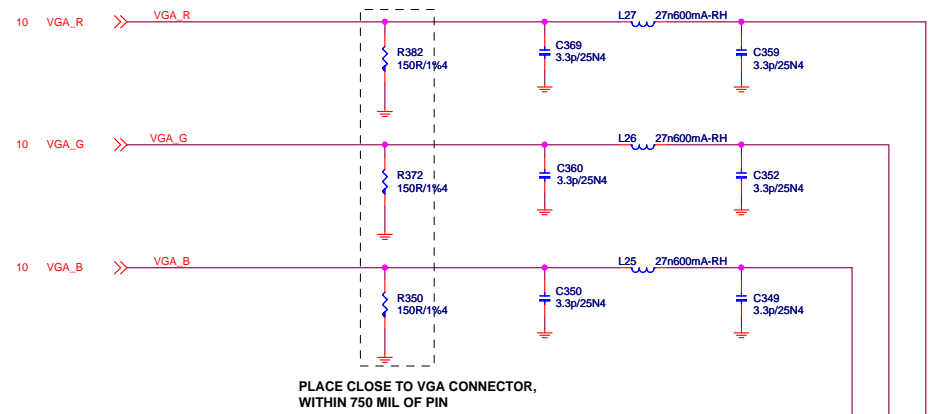
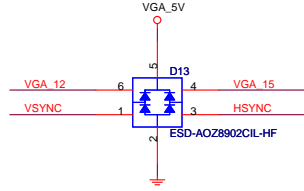
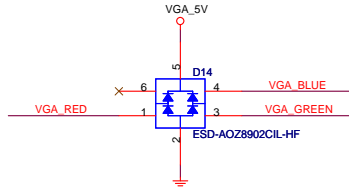
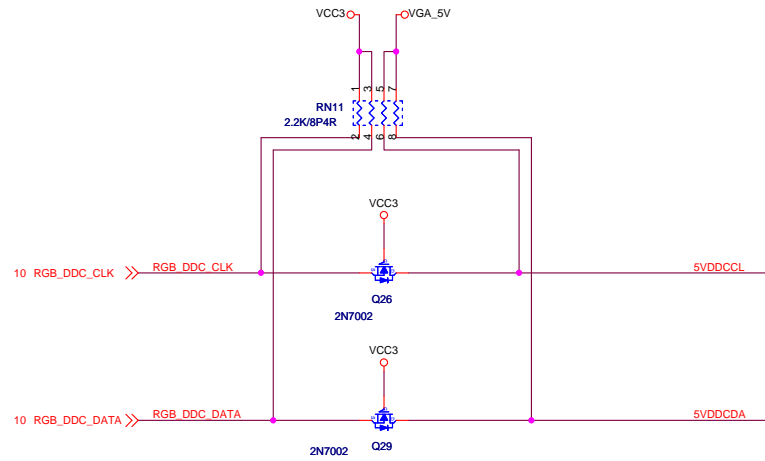
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Size Custom Document Description **HDMI Connector** Rev 20

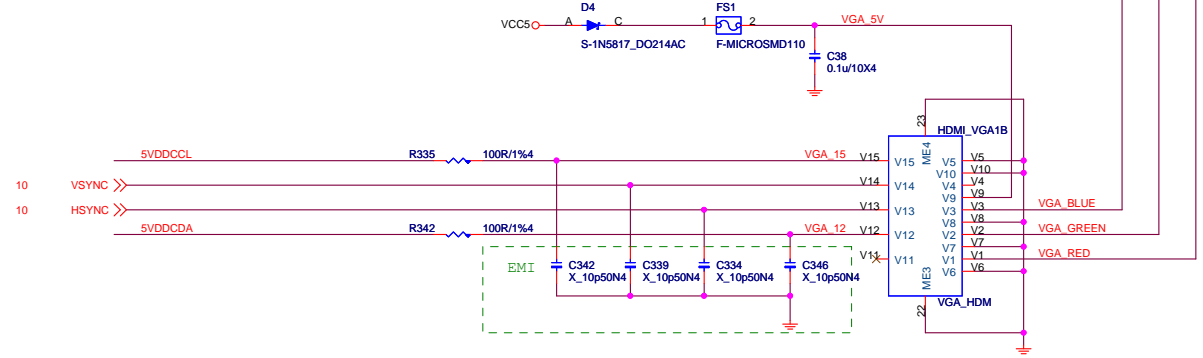
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D-Sub

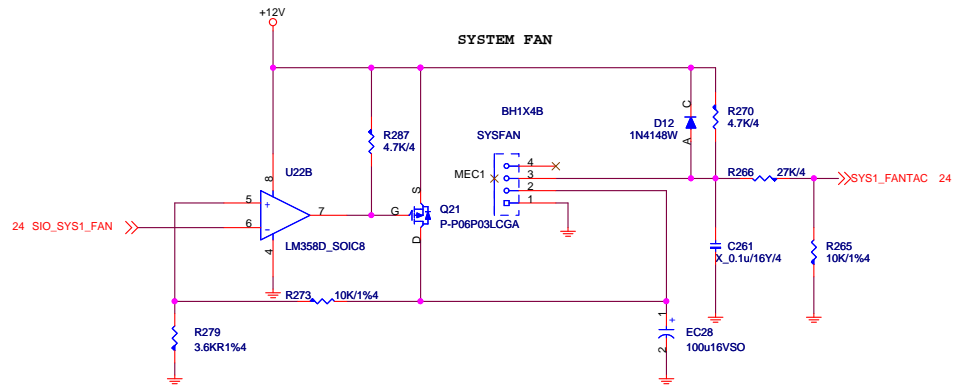
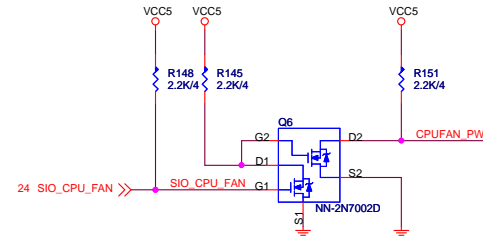
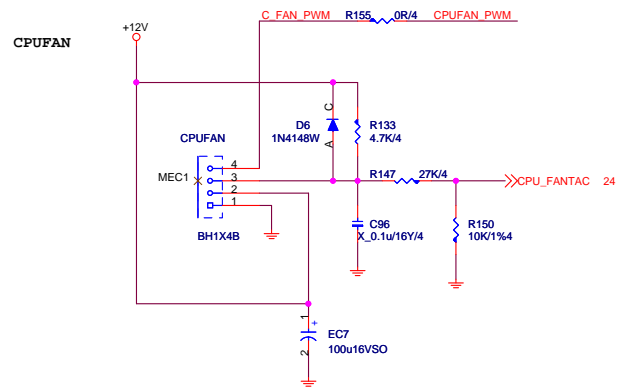
Level shift



PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN



FAN-COUNTROL CIRCUIT

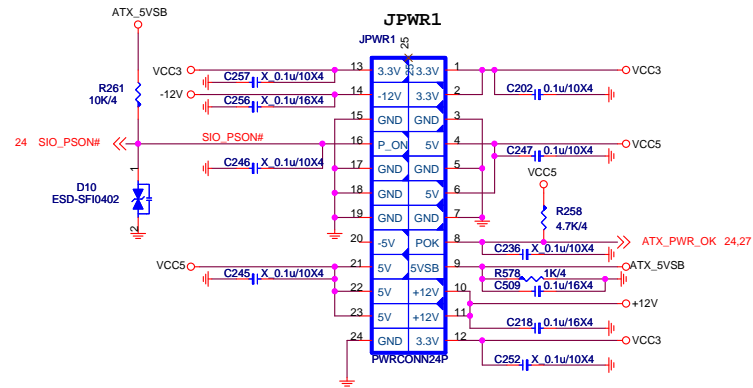


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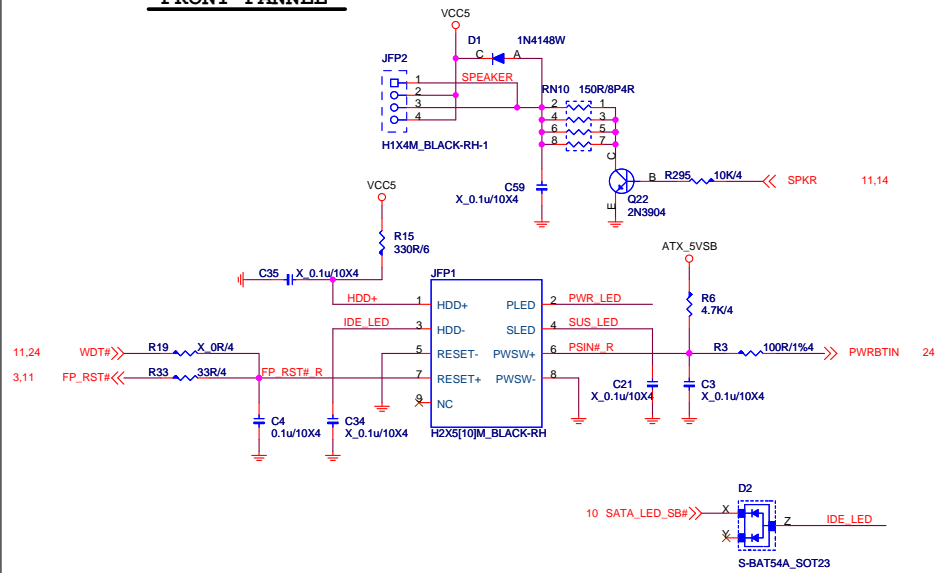
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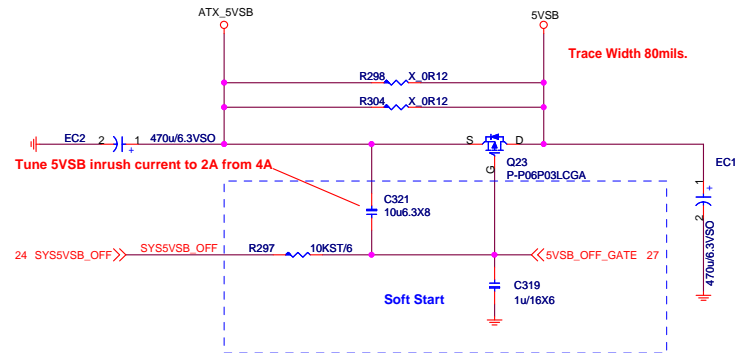
ATX POWER CONNECTOR



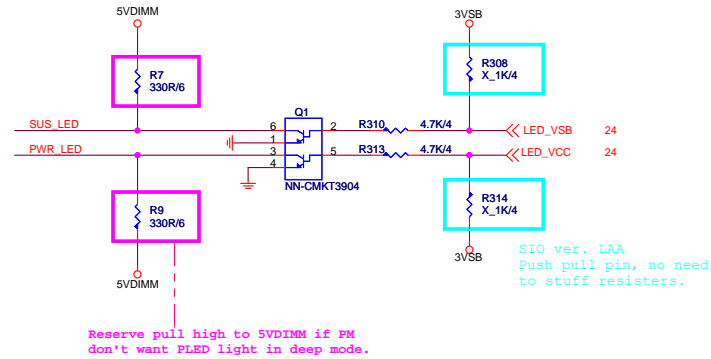
FRONT PANNEL



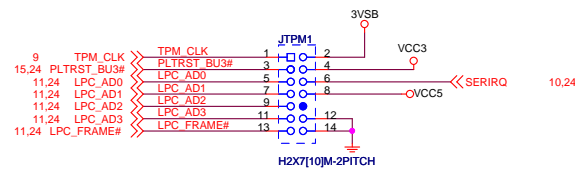
5VSB Power Switch



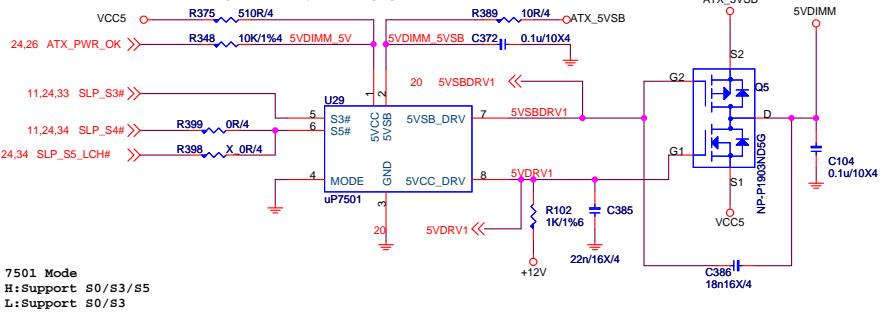
LED (for Fintek 71889)



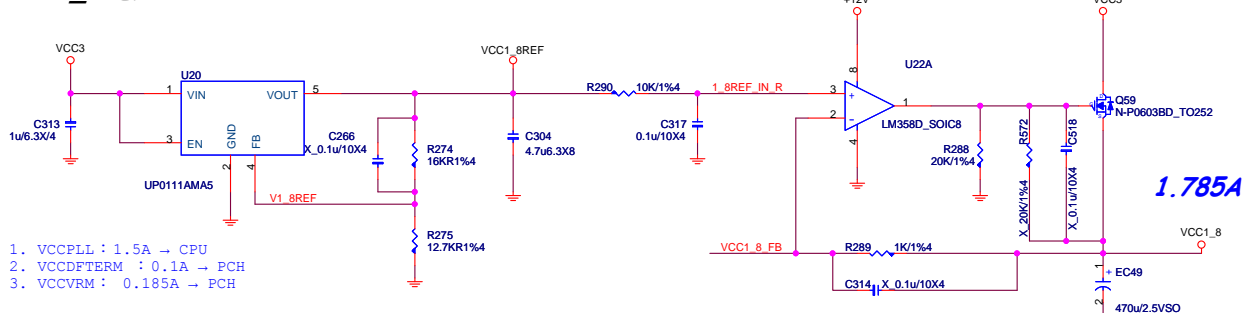
TPM



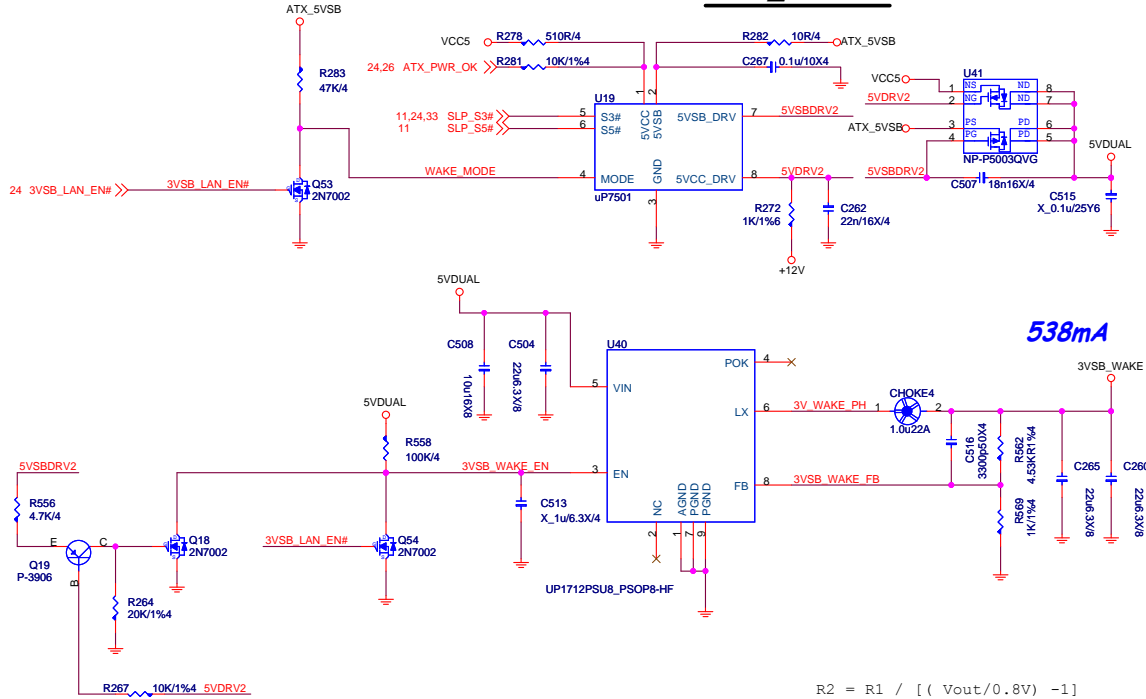
5VDIMM FOR DDR



VCC1_8REF

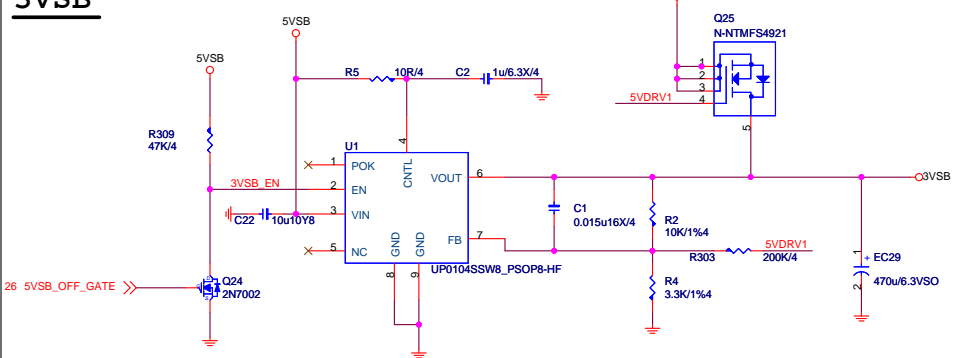


3VSB_WAKE



3VSB

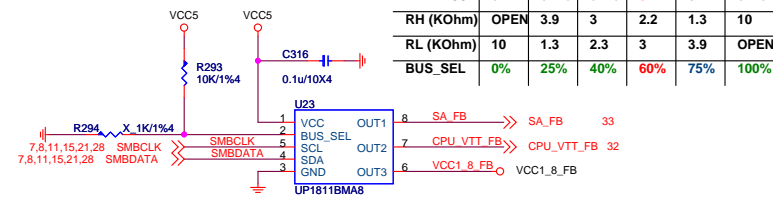
$$0.146A + \text{Mini PCIE } 1.5A = 1.646A$$



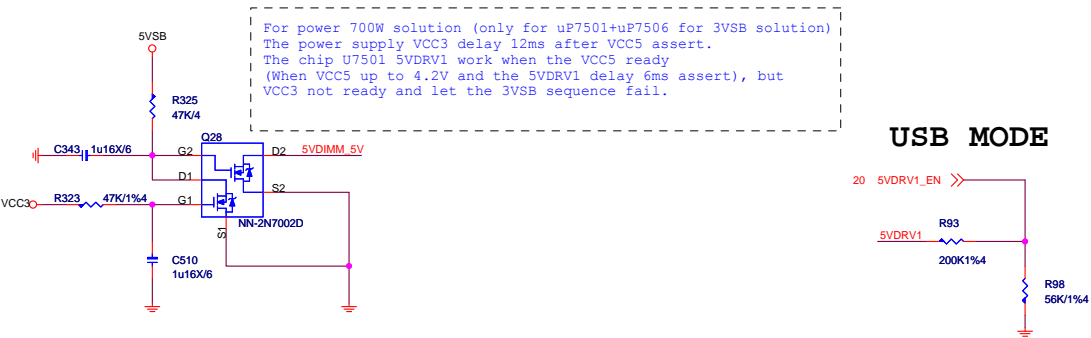
UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

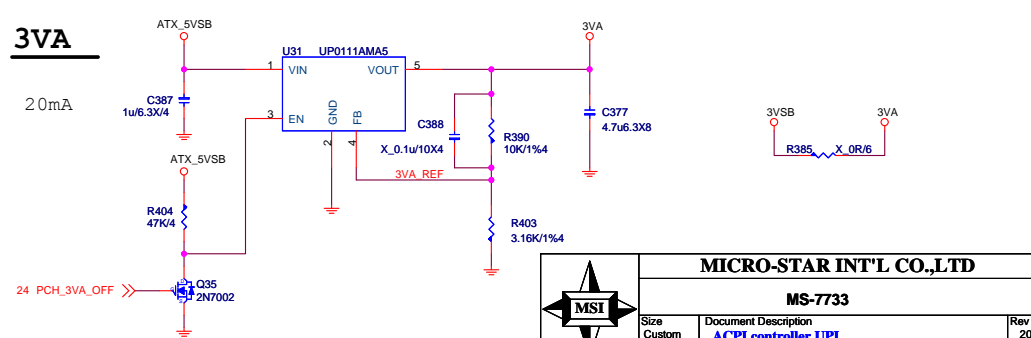


USB MODE



3VA

20mA



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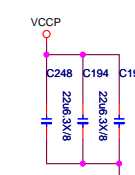
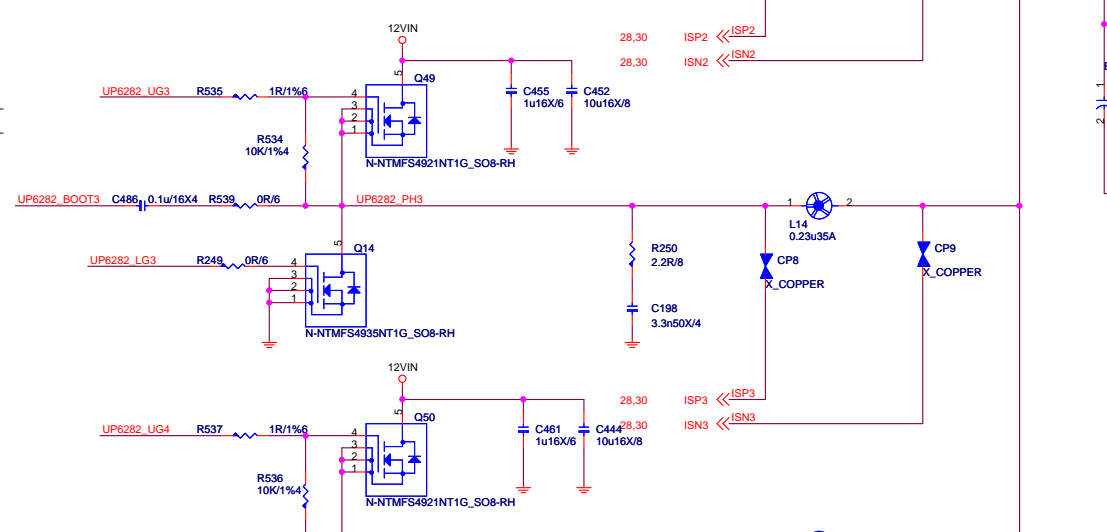
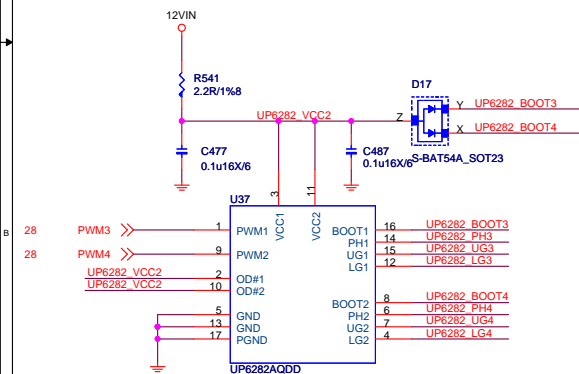
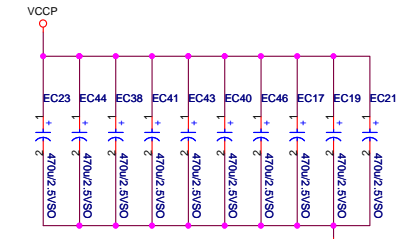
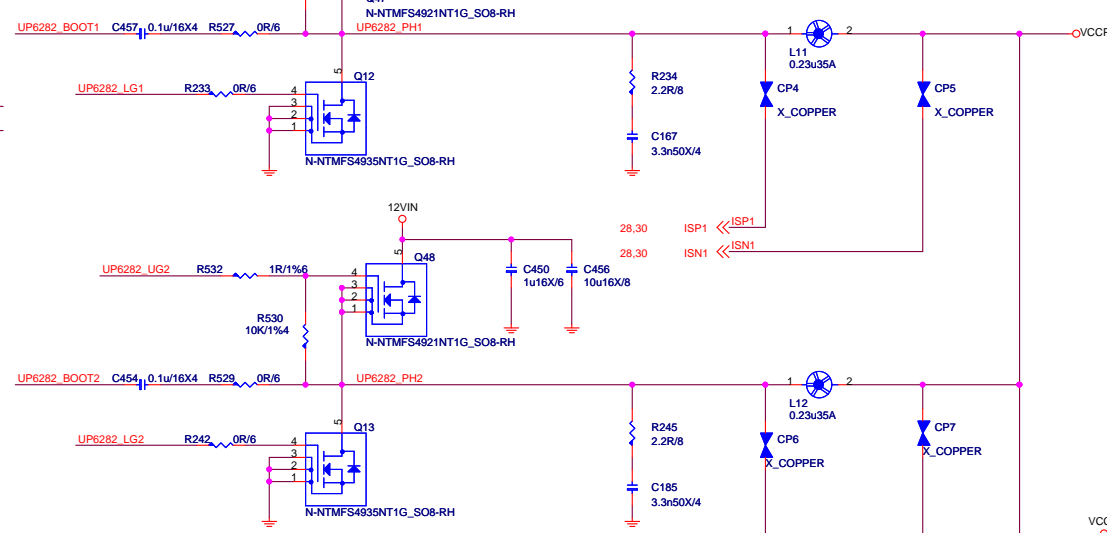
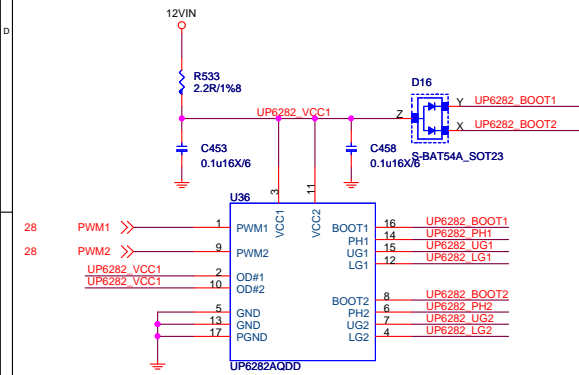
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Size	Document Description
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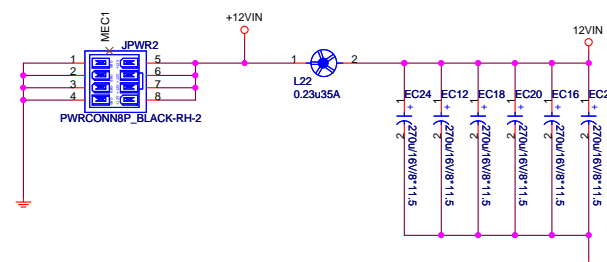
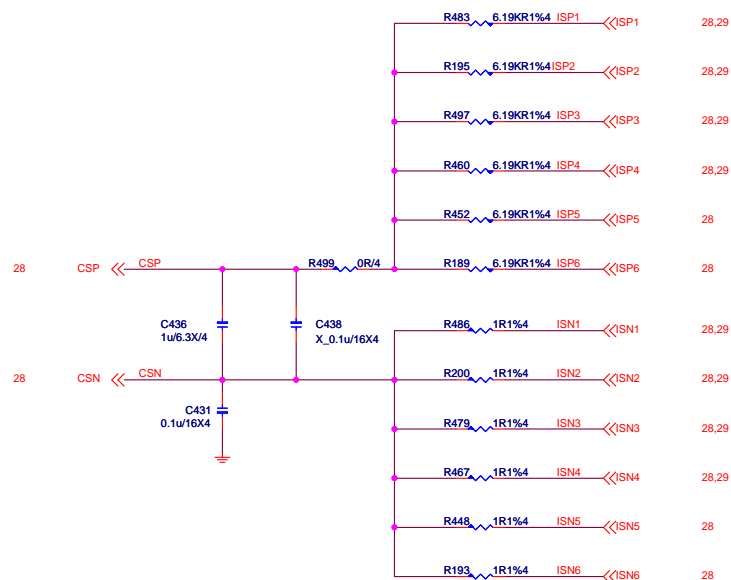
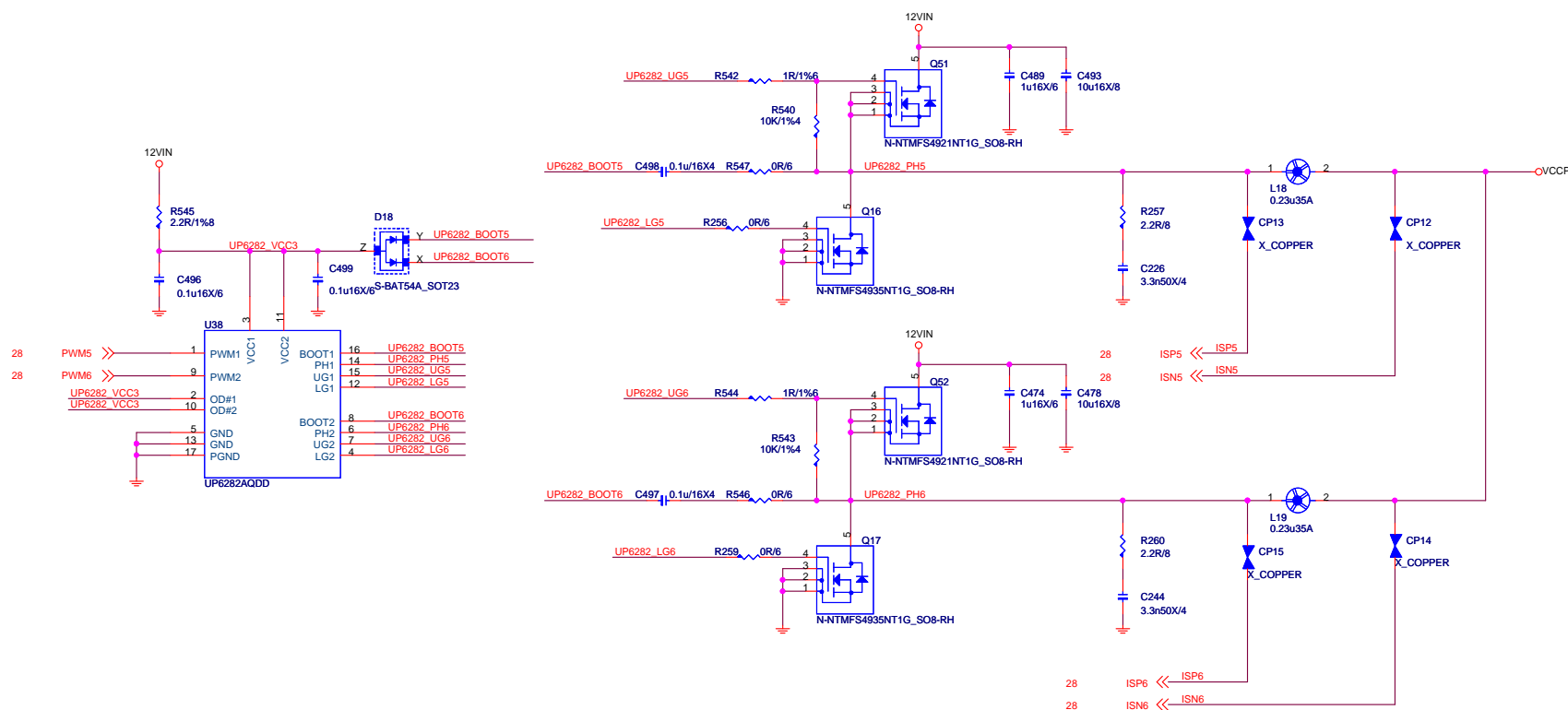
Rev	20
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0.5V~1.6V/110A

VCORE 112A TDC:85A
Per phase OCP=60A
LL:1.7m ohm



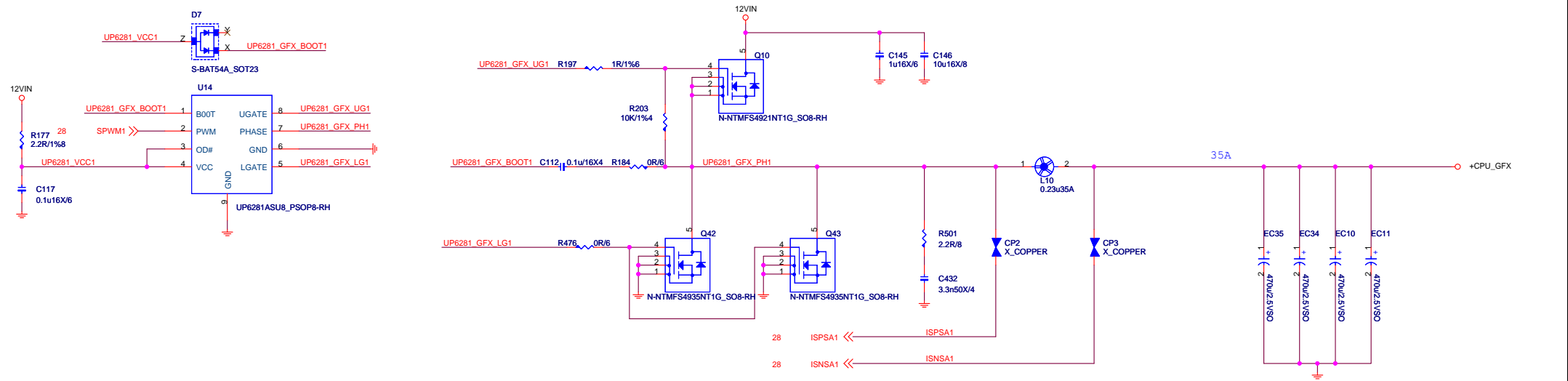
VCORE 112A TDC:85A
Per phase OCP=60A
LL:1.7m ohm



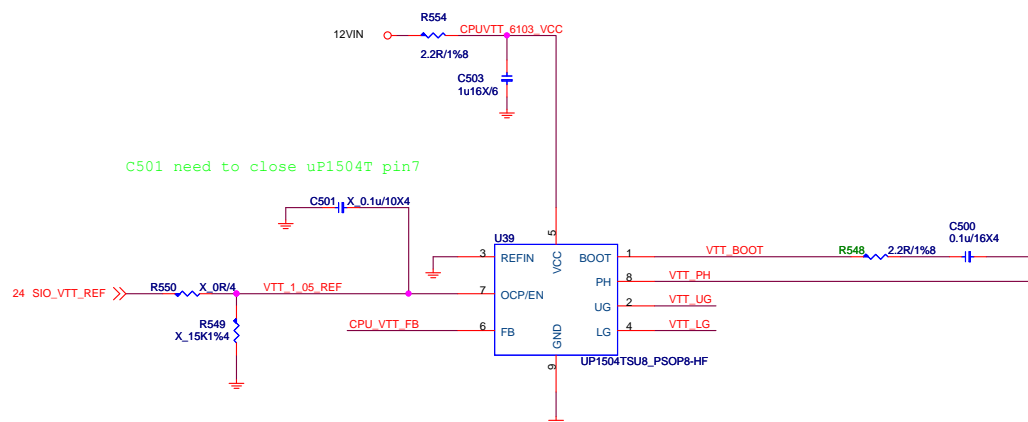
CPU_GFX:0.25-1.52

35A FOR CPU

OCP:60A



8.5A FOR CPU



3 VTT_SELECT_SIO

suggest 1.5V
max : 1.8V

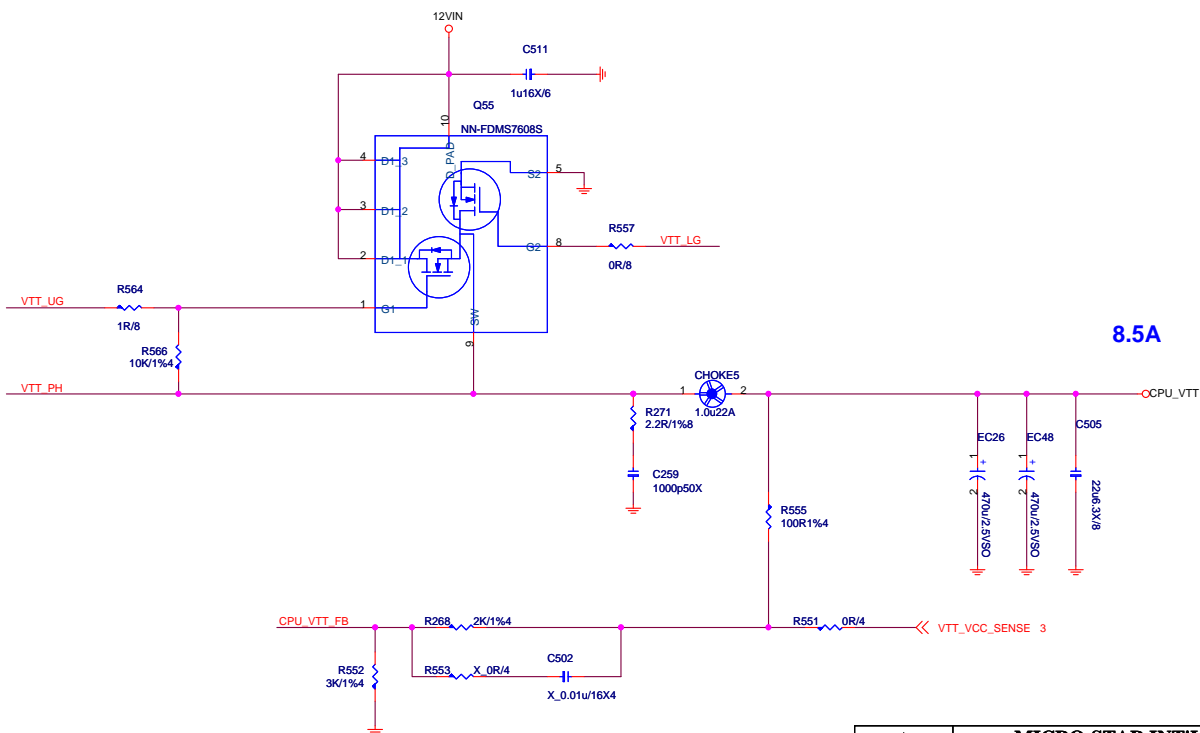
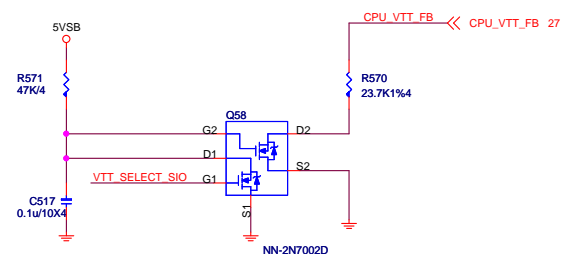
VCC5 CPU_VTT 5VSB

R453 10K/1%4 R455 X_1K/4 R567 20K/4 R450 4.7K/4

R462 4.7K/4

Q39 2N3904

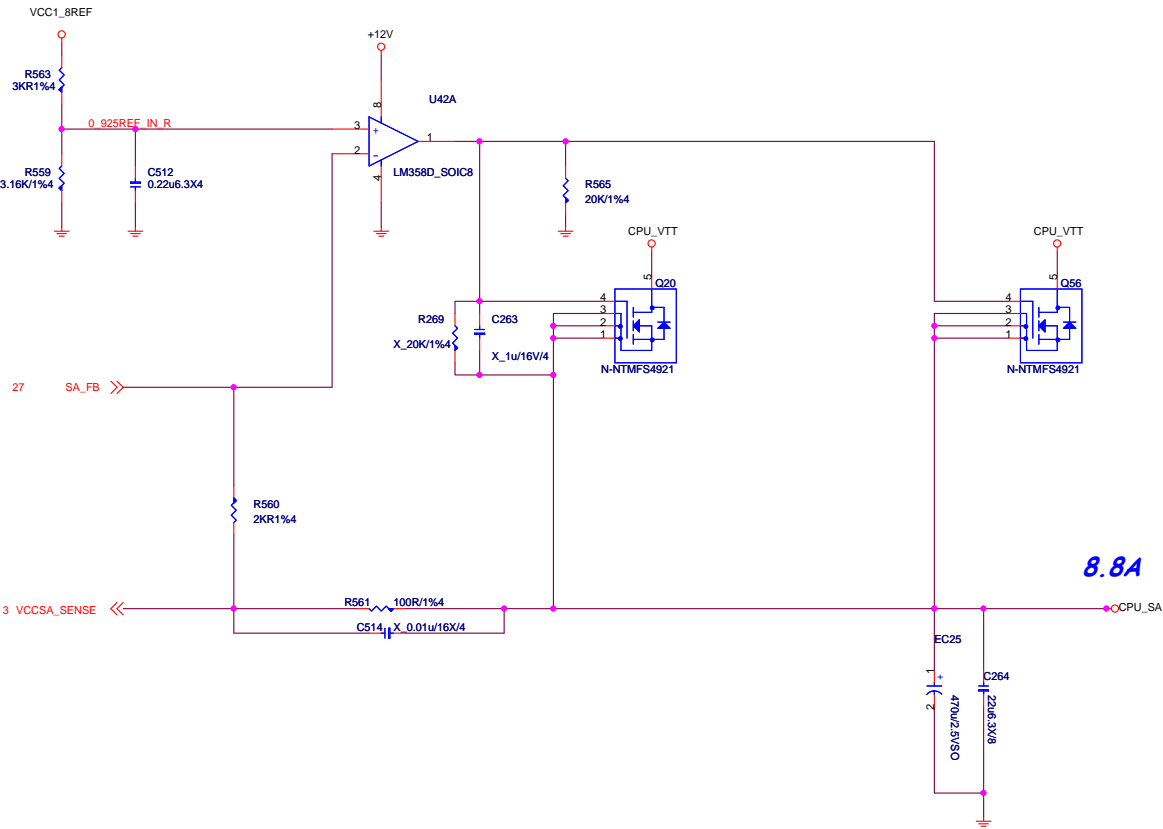
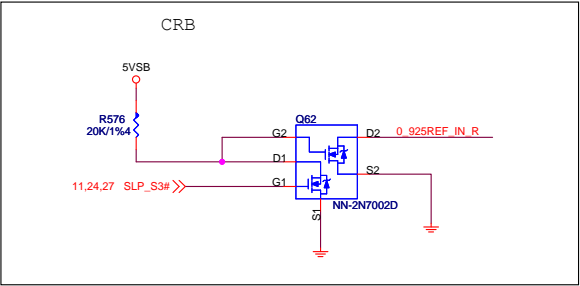
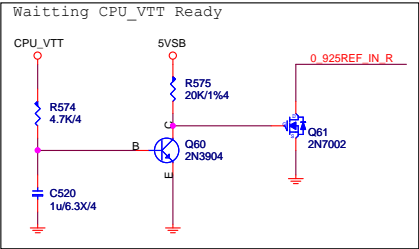
VTT_SELECT_SIO VTT_SELECT_SIO 24



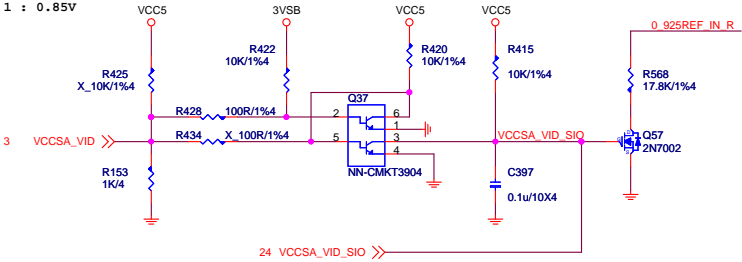
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CPU_SA:0.925/0.85
SA Core =8.8A



VCCSA_VID
0 : 0.925V
1 : 0.85V



DDR Power:1.5V

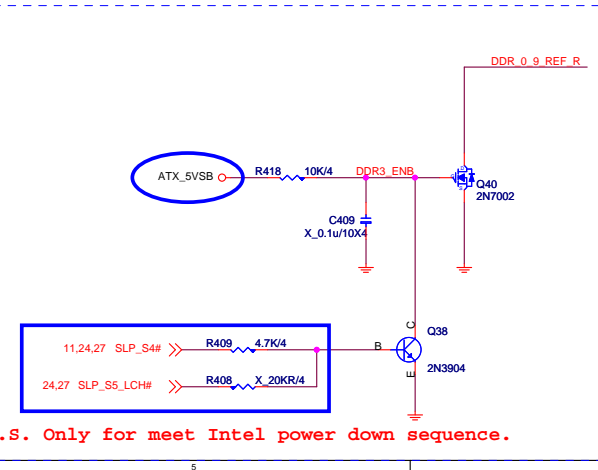
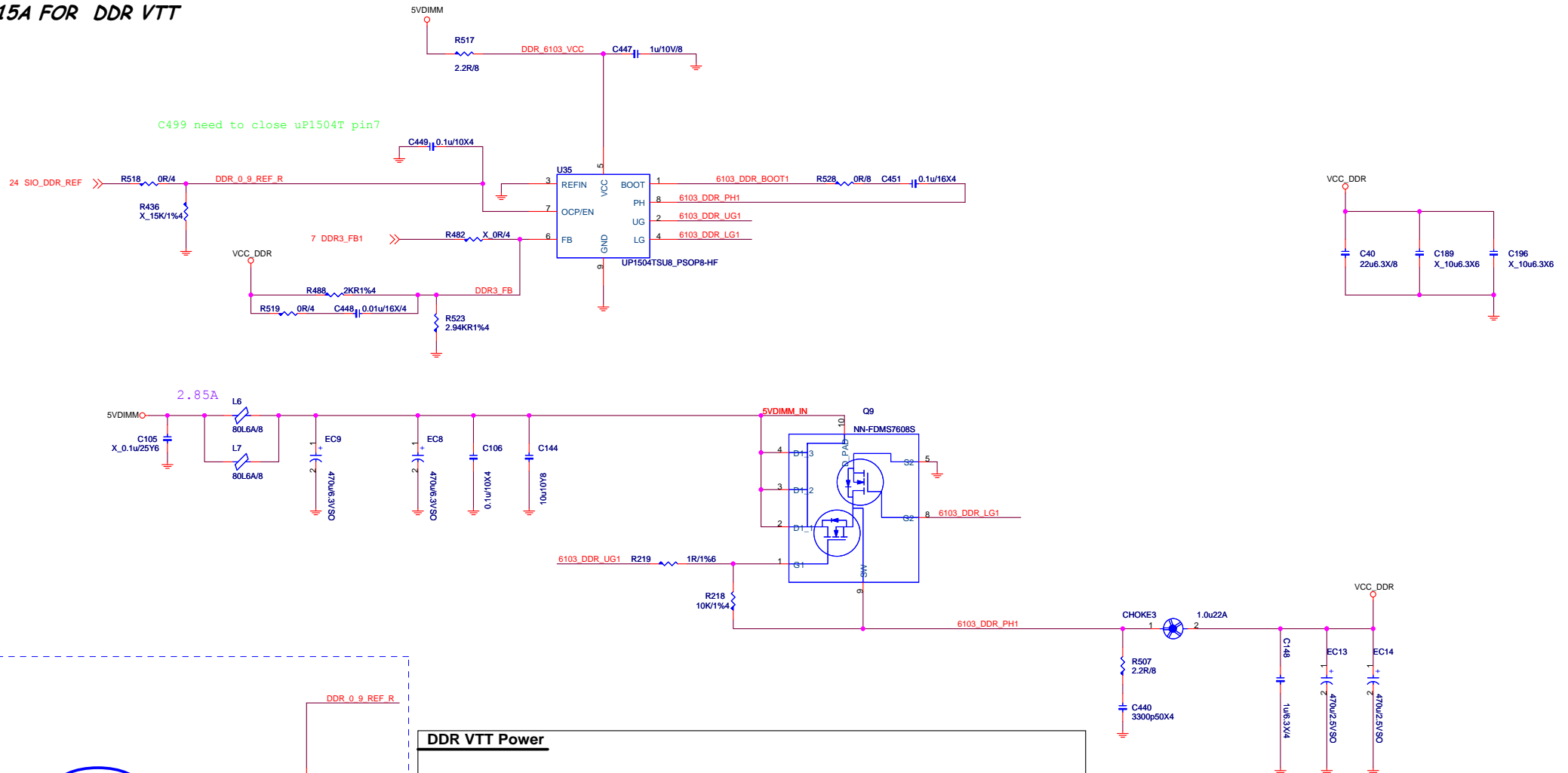
OCP:51.66A

DDR3_1.5V 4.75A+7.5A+0.415A=12.665A

4.75A FOR CPU

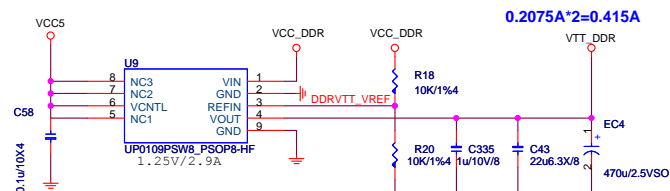
7.5A FOR 2DIMM

0.415A FOR DDR VTT



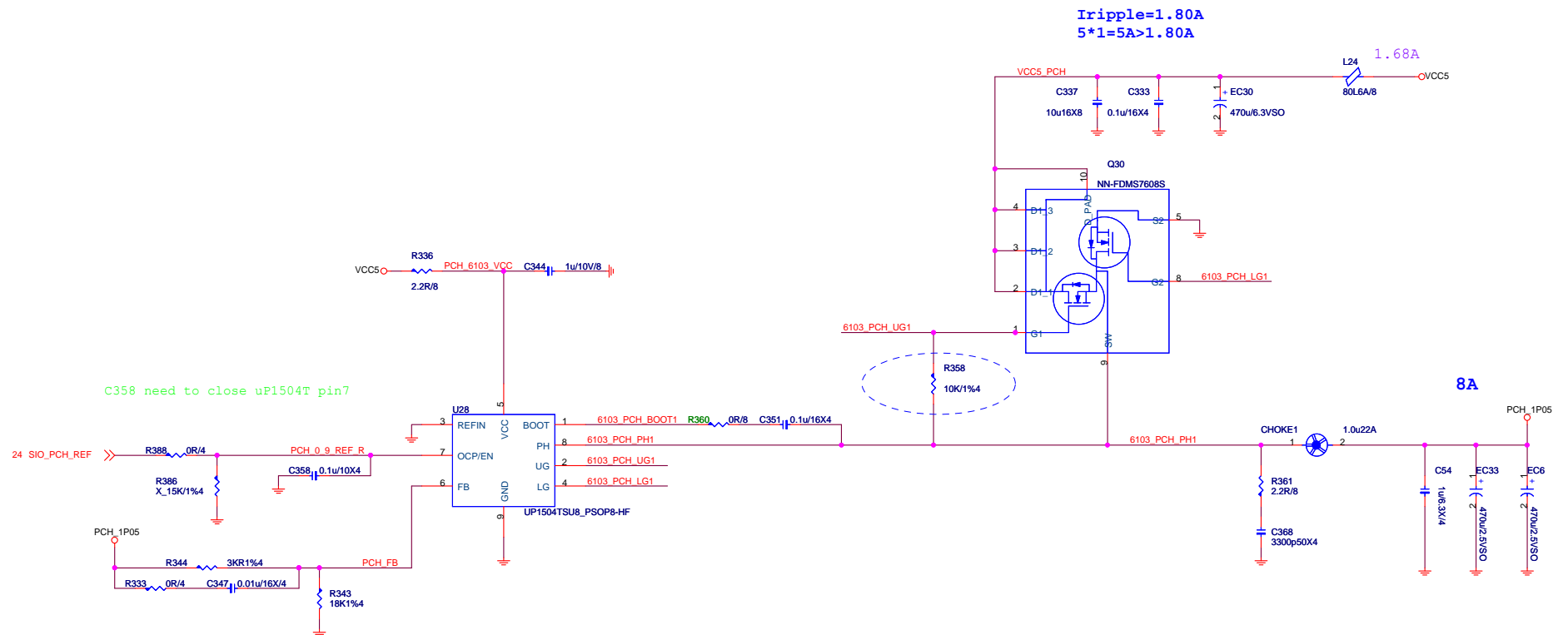
DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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OCP: 51.66A

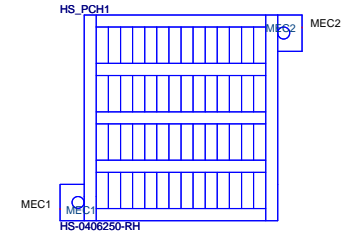
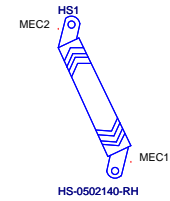


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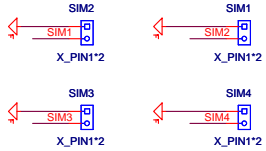
Size Custom	Document Description PCH Power - uP6103 1-Phase	Rev 20
Date: Thursday, July 05, 2012		Sheet 35 of 40



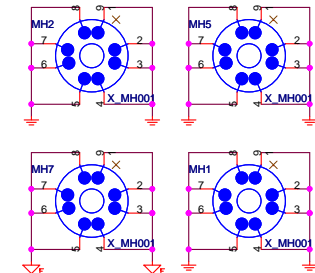
2012/5/112012/5/18PD0-0773320-G37,精成,23,寶安恩斯邁廠(MSIS)
2012/5/112012/5/18PD0-0773320-G37,精成,2,寶安恩斯邁廠(MSIS)
2012/5/112012/5/18PD0-0773320-E48,競華,23,寶安恩斯邁廠(MSIS)
2012/5/112012/5/18PD0-0773320-E48,競華,2,寶安恩斯邁廠(MSIS)



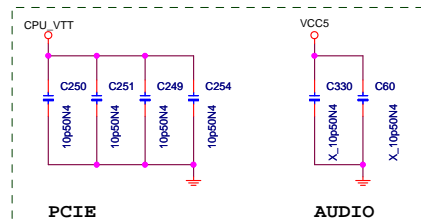
Simulation



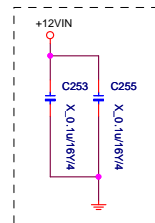
Mounting Holes



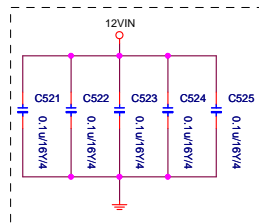
EMI:cap. for signal return path



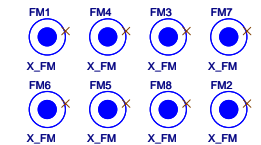
EMI



Close to L23



Optical Fiducial Marks-120



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